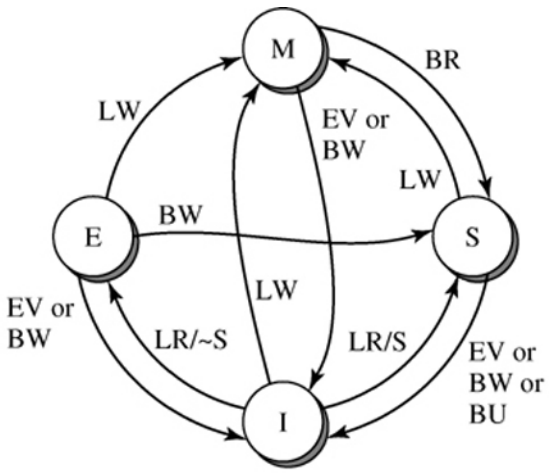
MESI Cache Coherence Protocol

State Table (s' = next state)

- view from local cache to local events (LR,LW,EV) and bus events (BR,BW,BU)

Current State s	Local Read (LR)	Local Write (LW)	Local Eviction (EV)	Bus Read (BR)	Bus Write (BW)	Bus Upgrade (BU)
Invalid (I)	Issue bus read; if no sharers s'=E else s'=S	Issue bus write s'=M	s'=I	Do nothing	Do nothing	Do nothing
Shared (S)	Do nothing	Issue bus upgrade s'=M	s'=I	Respond shared	s'=I	s'=I
Exclusive (E)	Do nothing	s'=M	s'=I	Respond shared s'=S	s'=I	Error
Modified (M)	Do nothing	Do nothing	Write data back; s'=I	Respond dirty; Write data back s'=S	Respond dirty; Write data back s'=I	Error

State Diagram



In response to local and bus events the coherence controller may need to change the local coherence state of a line, and may also need to fetch or supply the cache line data.

Figure 11.5 from Modern Processor Design

Directory MSI Protocol

Nodes

- local: contains cache generating request
- home: contains requested memory block
- remote: contains cache with copy of memory block

Messages

Type	Source	Dest'n	Contents	Action
read miss	local cache	home directory	P,A	request data and make P sharer
write miss	local cache	home directory	P,A	request data and make P owner
upgrade	local cache	home directory	P,A	make P owner
invalidate	home directory	remote cache	A	invalidate copy
fetch	home directory	remote cache	A	remote cache send data to home directory and set shared
fetch/ invalidate	home directory	remote cache	A	remote cache send data to home directory and invalidate
data reply	home directory	local cache	A,D	return data from home directory
data writeback	remote cache	home directory	A,D	writeback modified data at address A

Contents

- P = processor number
- A = address
- D = data

Example: initially processors P1, P2, and P3 share block B1. Then (step 1) P1 writes B1. Then (step 2) P2 reads B1.

Snooping with MESI:

Step	Bus Transaction		B1 state		
	Request	Snoop Response	P1 cache	P2 cache	P3 cache
0	-	-	S	S	S
1	P1:upgrade	-	M	I	I
2	P2:read miss P1: writeback	P1:dirty	S	S	I

Directory with (M)odified, (S)hared, (U)ncached states (MSI in cache):

Step	Message			B1 state				
	Sender	Recipient(s)	Type	HD Dirty	HD sharers	P1 cache	P2 cache	P3 cache
0	-	-	-	0	1 1 1	S	S	S
1	P1 HD	HD P2,P3	upgrade (P1,B1) invalidate (B1)	1	1 0 0	M	I	I
2	P2 HD P1 HD	HD P1 HD P2	read miss (P2,B1) fetch (B1) writeback (B1,data) data reply (B1,data)	0	1 1 0	S	S	I