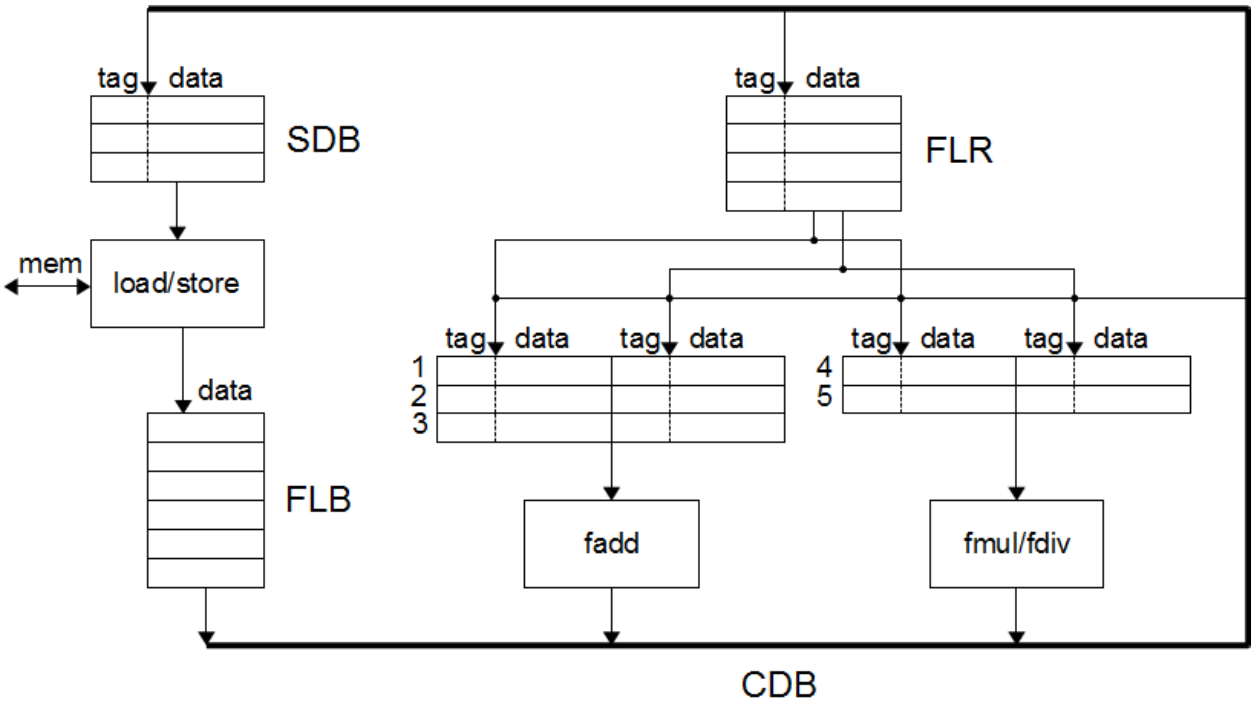
IBM 360/91 FPU



Sample Instruction Sequence

```
W: F4 <- F0 + F6
X: F2 <- F0 * F4
Y: F4 <- F4 + F6
Z: F6 <- F4 * F2
```

Register Contents

```
F0=6, F2=2, F4=10, F6=8
```

Assumptions (made to make execution trace shorter)

- Can dispatch 2 instructions in program order per cycle
- Execution starts in same cycle as dispatch
- Results communicated on CDB during last cycle of execution
- fadd is pipelined (2 stages), fmul is pipelined (3 stages)

Cycle	FADD RS	tag	data	tag	data	unit	FMUL/DIV RS	tag	Data	tag	data	unit	FLR	tag	data
1	1						4						F0		
	2						5						F2		
	3												F4		
													F6		
2	1						4						F0		
	2						5						F2		
	3												F4		
													F6		
3	1						4						F0		
	2						5						F2		
	3												F4		
													F6		
4	1						4						F0		
	2						5						F2		
	3												F4		
													F6		
5	1						4						F0		
	2						5						F2		
	3												F4		
													F6		
6	1						4						F0		
	2						5						F2		
	3												F4		
													F6		
7	1						4						F0		
	2						5						F2		
	3												F4		
													F6		
8	1						4						F0		
	2						5						F2		
	3												F4		
													F6		
9	1						4						F0		
	2						5						F2		
	3												F4		
													F6		