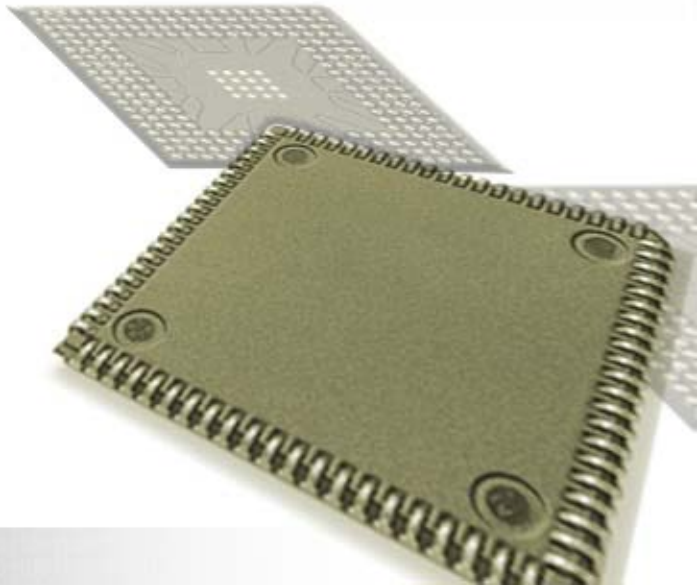
XILINX®

Digital Cinema

"The mission of Xilinx is
to help our customers
attain the fastest time-to-market
and flexible product life cycle
management through programmable
logic solutions consisting of
software, silicon and support."

Wim Roelandts
President and CEO



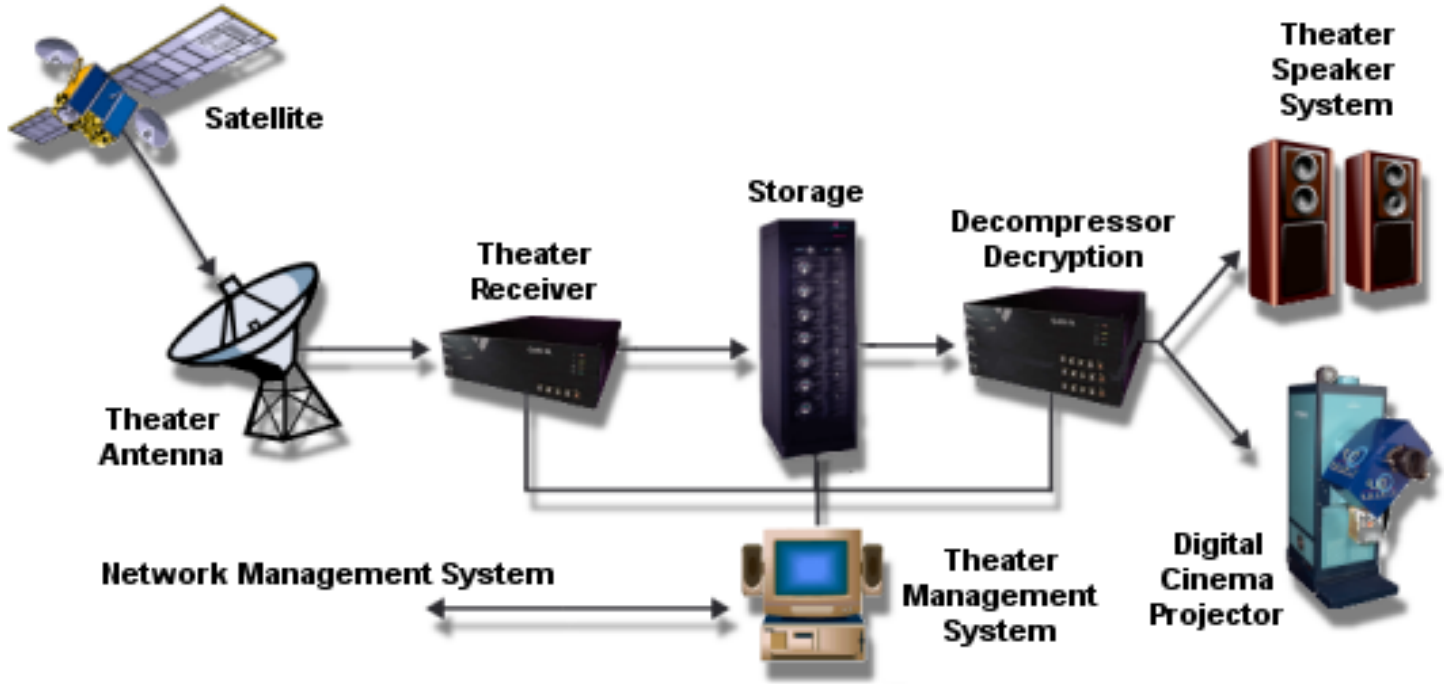
esp
EMERGING STANDARDS
& PROTOCOLS

Agenda

- Introduction and market overview
- The industry today
- System overview
  - Xilinx solutions and how we add value
- Summary

What is Digital Cinema?

- Digital Cinema is a complete system to deliver ”cinema-quality" programs to “theaters” (including consumer homes) throughout the world using digital technology



Market Overview

- Only 100,000 cinema screens worldwide, with about 6,000 new screens replaced and added per year
  - Large venue theaters not a large market but high value products used
  - “Entertainment industry to spend $3 billion by 2005 to convert 21,000 theaters to digital” (SRI Consulting, May 2000)
  - Adaptation of existing technologies is widespread
- A market for companies to showcase image processing and display capabilities to cinema-goers (consumers)
  - They might consider similar technologies for their home theatre systems

Why Go Digital?

- Directors
  - The director's vision can now actually be seen by audiences
  - Post-production can all be done digitally (no film transfers)
- Distributors
  - Duplication costs removed
  - Better piracy prevention
  - Larger numbers of theatres can now view simultaneously
  - Transportation costs can be replaced by much lower transmission costs
- Exhibitors
  - More flexible scheduling (e.g. more simultaneous screenings)
  - New entertainment ideas (e.g. lighting FX/aromas tied to film)
- Audiences
  - Higher quality entertainment (better picture and sound)
  - Easier access to screenings (more simultaneous showings)

Digital Cinema System Overview

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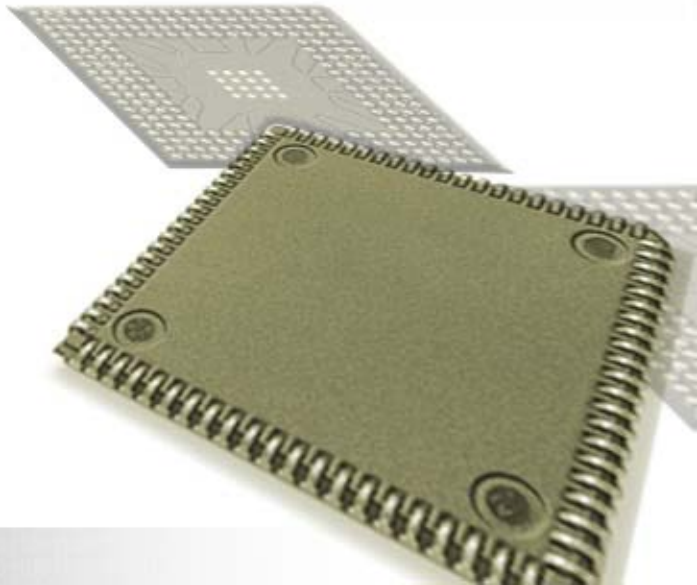
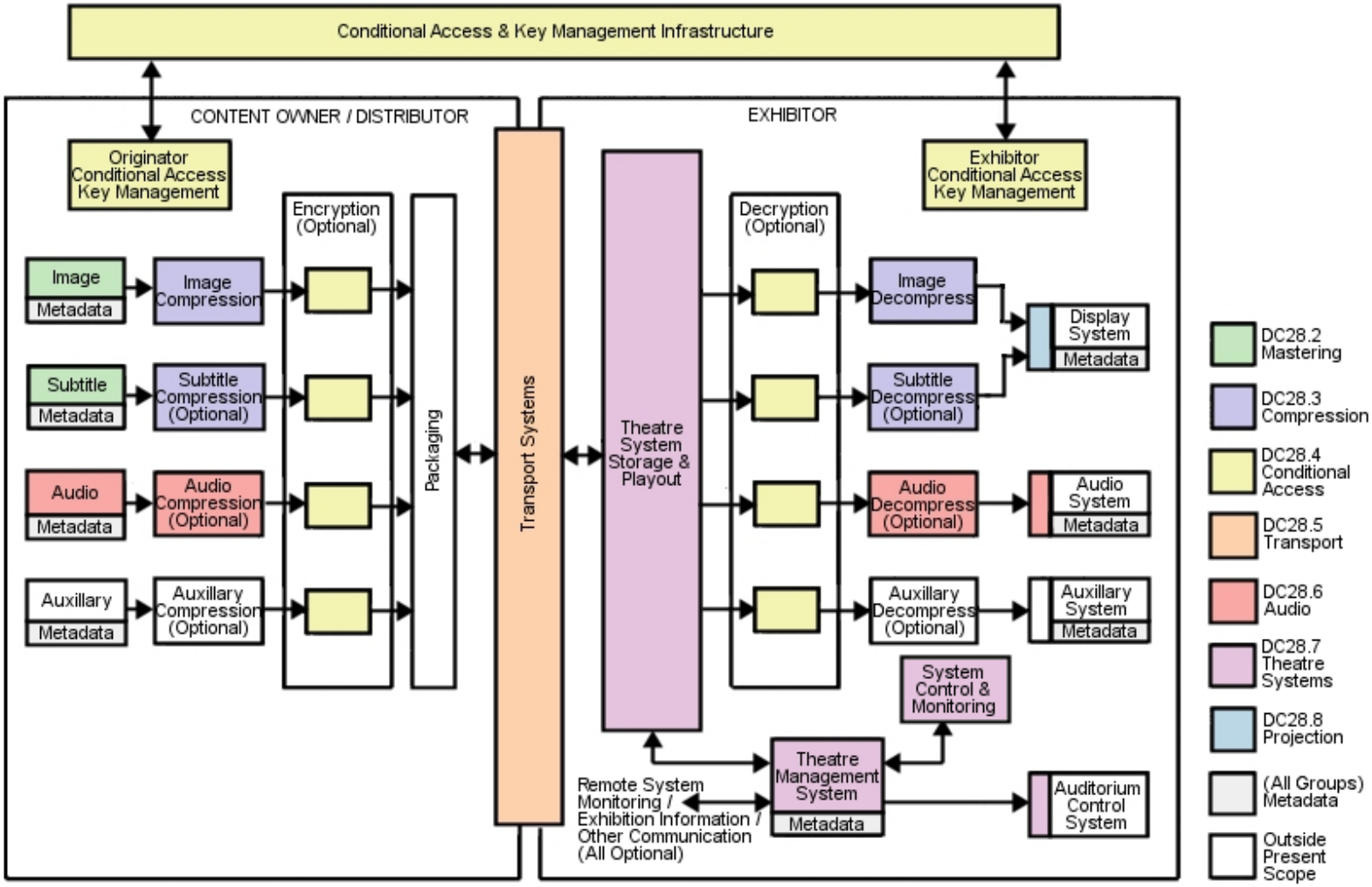


SMPTE DC28 System



Courtesy: SMPTE

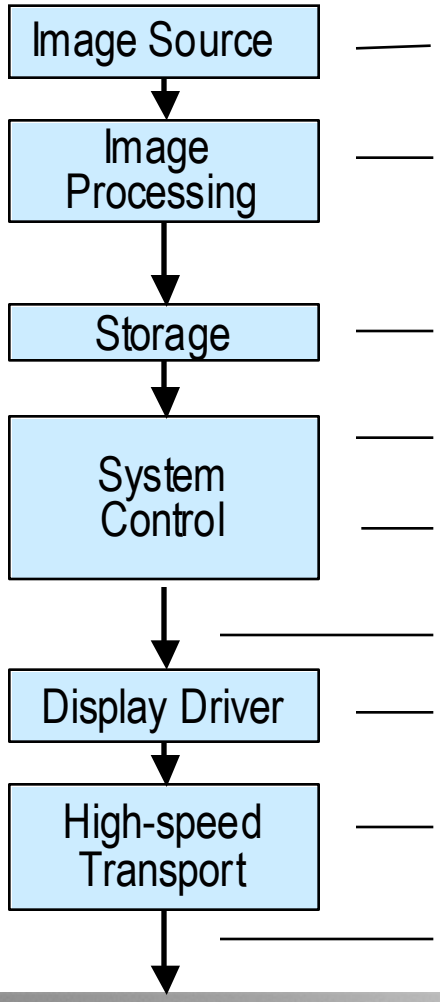
SMPTE DC28 System

- SMPTE (Society Motion Picture and TV Engineers) is active in the standardization of and interoperability between all blocks in the chain
- DC28 is SMPTE subcommittee focused on D-Cinema
- All aspects of capture, process, display and transport need to be addressed to ensure market adoption
- D-Cinema is much more than just projection!
- Xilinx devices can be used in most parts of the chain

Image Capture

- Professional Digital Camcorder
  - Outputs digital RGB images which can be digitally processed directly in post-production
- Standard Film Camera
  - Requires telecine conversion
    - Scans film electronically to produce very high definition digital images
    - High performance image processing and high bandwidth capabilities provided by Xilinx FPGAs ideal for telecine applications
    - Various high speed network interfaces to/from telecine also possible with Xilinx IP and cores

Digital Image Capture System Data Flow



CCD through A/D conversion
- Captured raw digital RGB values of analog image from CCD

Image Processing
- DCT/IDCT, color space conversion, compression, etc.
- Gamma/color correction, half-toning, brightness, contrast, sharpness, etc.

Nonvolatile Storage
- Compact FLASH, Hard Disk Drive, CD-R interfaces

System Controller
- Hardware I/O & memory decoding, synchronization, status, interrupts, etc.

Microcontroller
- Scheduler, task mgr., resource allocator, menu mgr., etc.

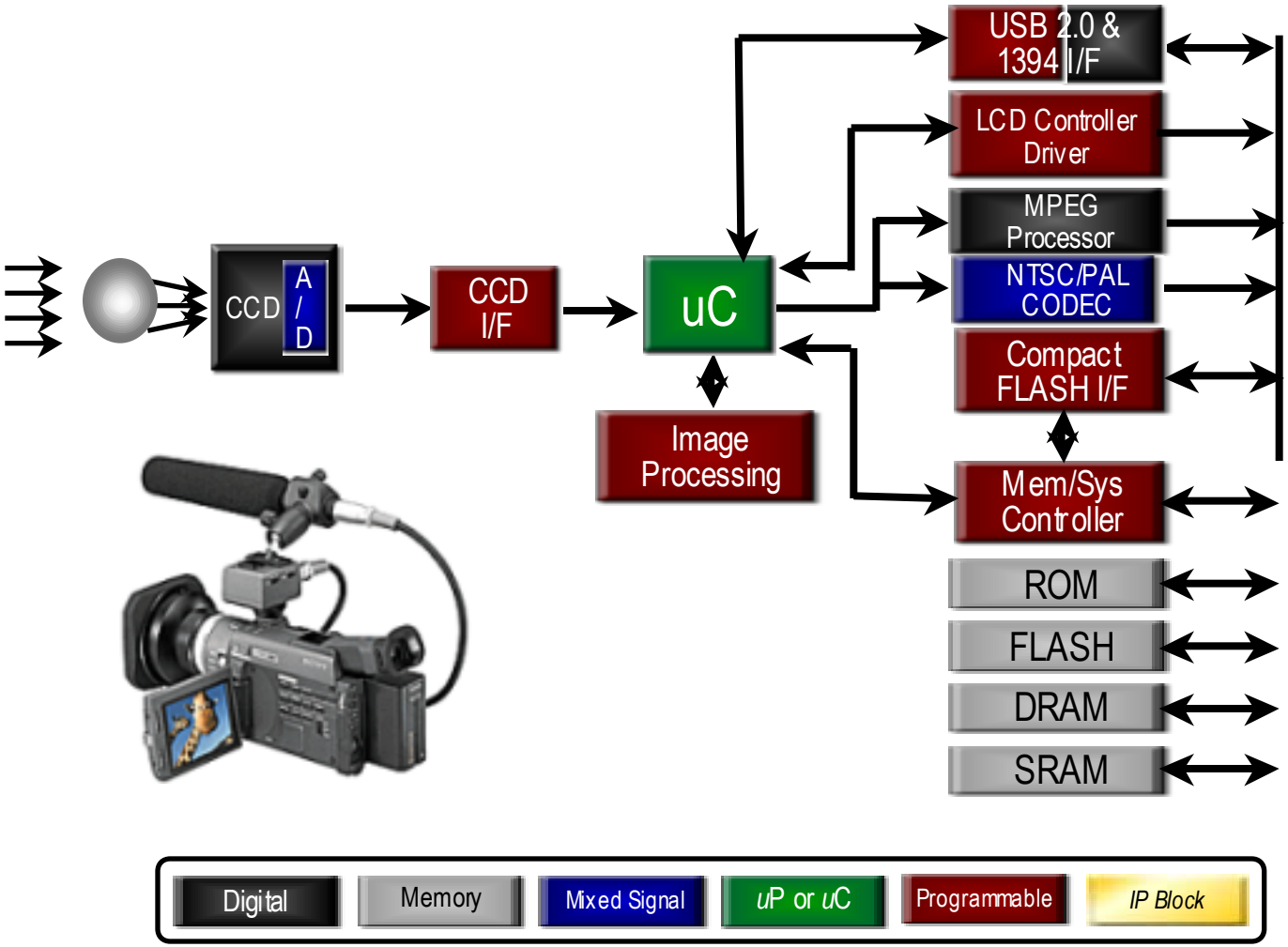
System Transport
- DMA access to system memory resources, PCI, local bus, dual-port memories

LCD Display
- Timing control, frame rate controller, Select I/O

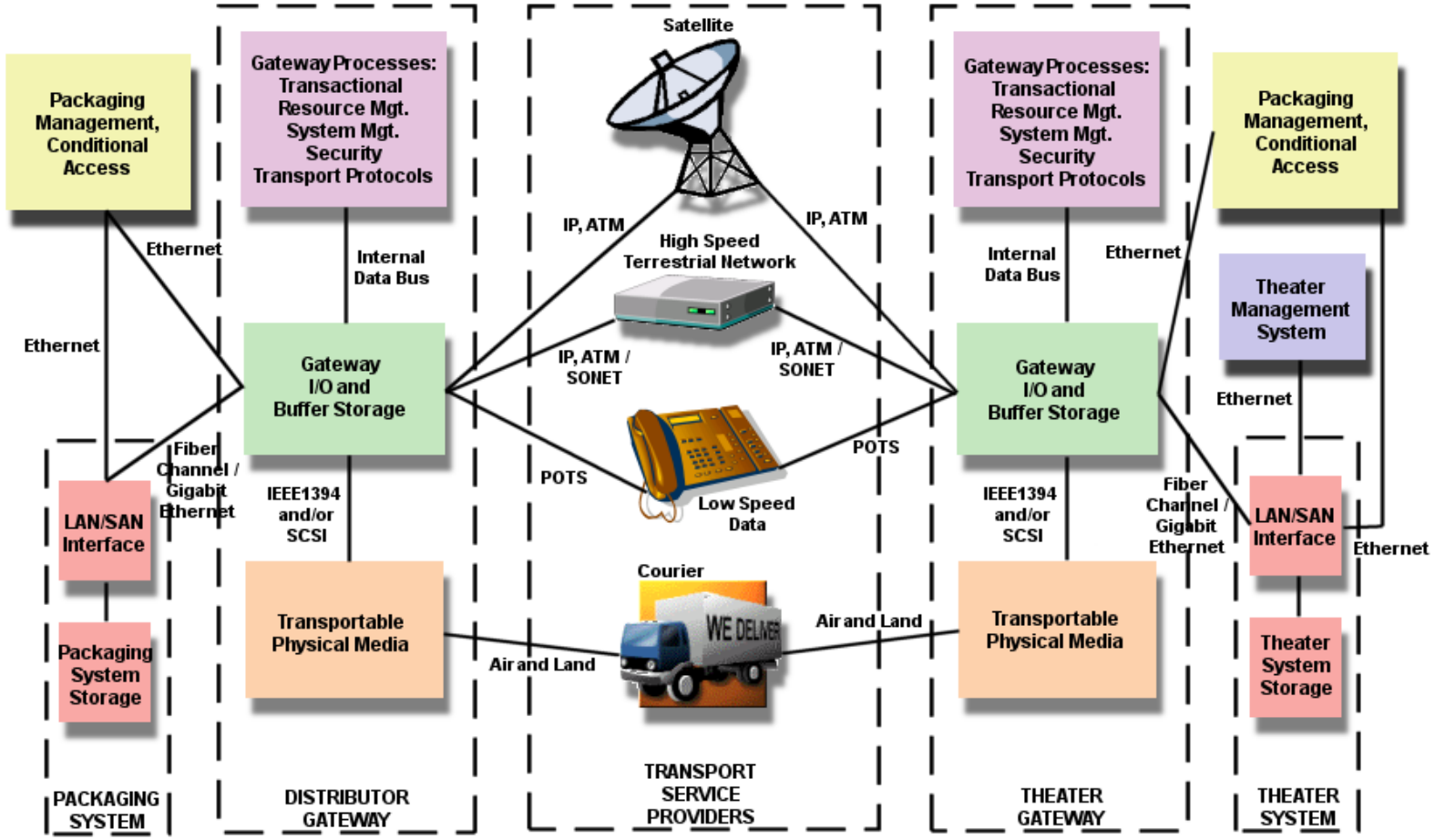
Fast Image Distribution
- USB 2.0, IEEE-1394, Ethernet MACs

PHY
- LVDS, BLVDS

Digital Video Camera Diagram



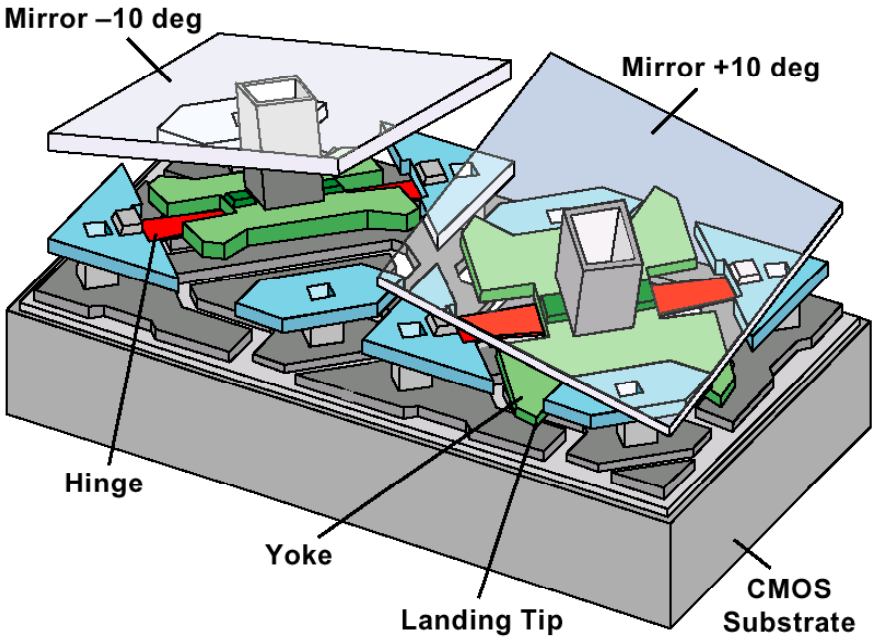
Transport System



Projection Technologies

- DLP - Digital Light Processor
- DMD - Digital Micromirror Device
- AMLCD - Active Matrix Liquid Crystal Display
- LCOS - Liquid Crystal On Silicon
- D-ILA - Direct Drive Image Light Amplifier
- GLV - Grating Light Valve

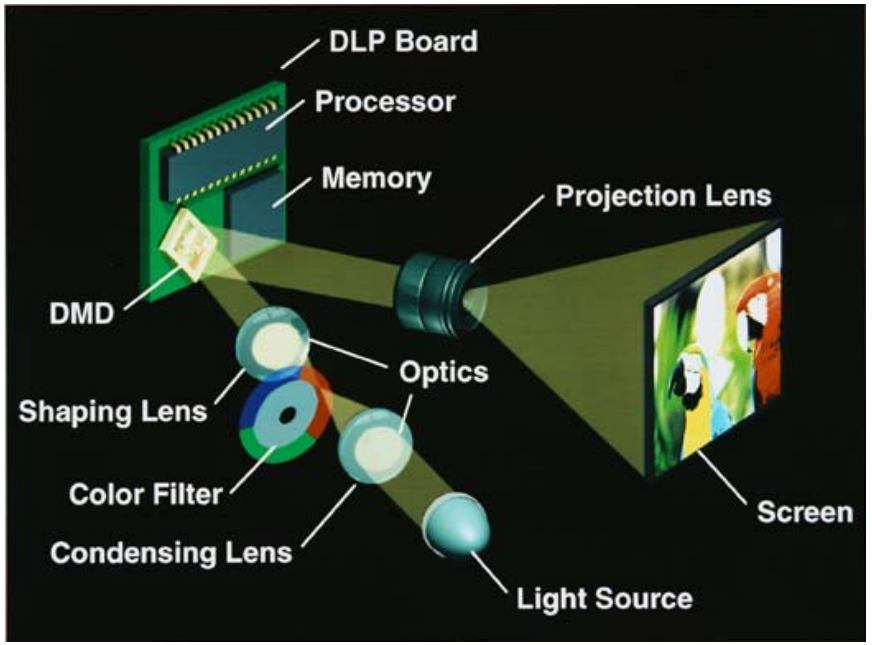
Texas Instruments DLP - DMD



- Digital Micromirror Device (DMD) is an array of 16µm^2 mirrors that tilt to an "on" or "off" position depending on underlying memory cell state
- Grayscale images can be built on array using binary pulse width modulation

TI DLP - Single DMD System

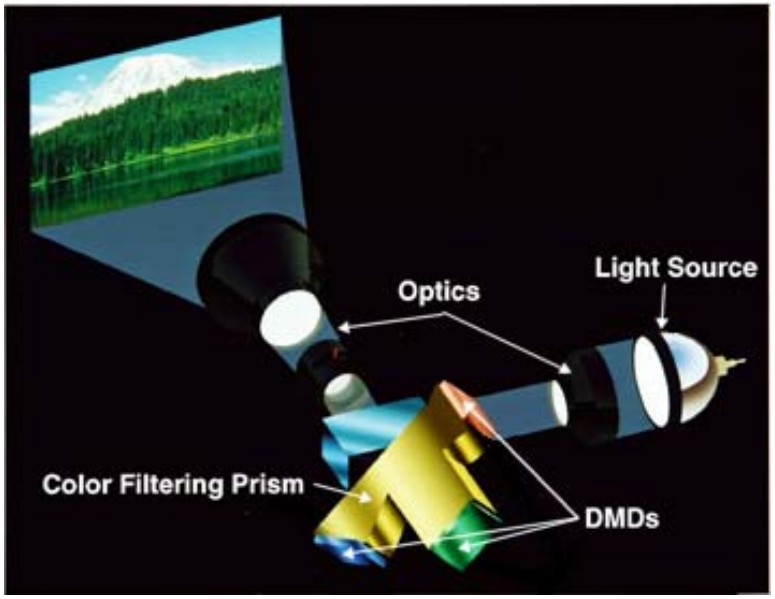
- Color images can be made by shining colored light onto DMD grayscale image
- Light from source bulb is filtered using spinning color wheel
- Combination of red, green or blue light is then reflected to optics from DMD



Courtesy of: Texas Instruments

TI DLP - 3 DMD System

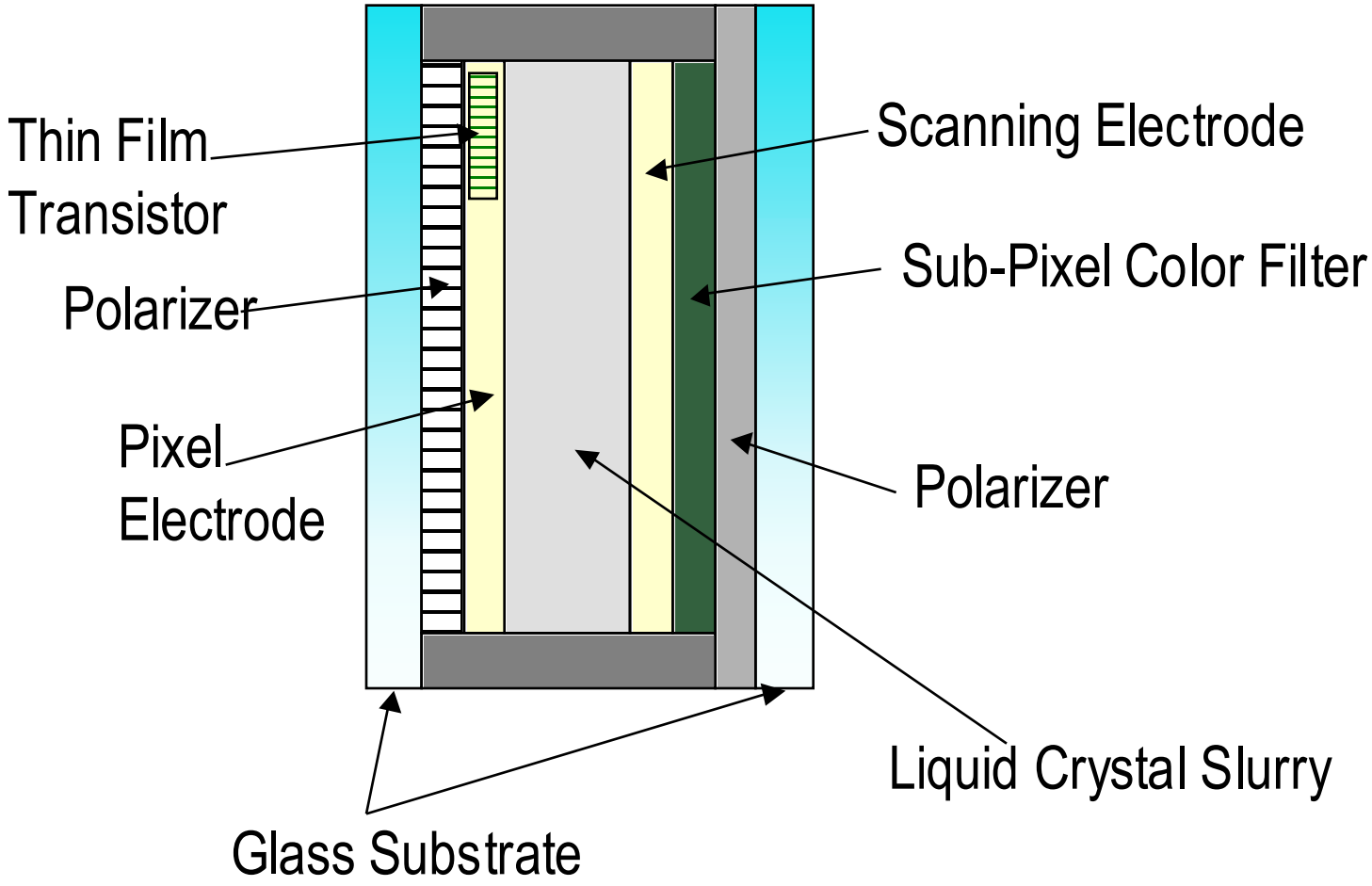
- Light from source bulb is diffracted using filtering prism
- Each color component (red, green and blue) is reflected from its own dedicated DMD
- Reflected R,G and B light combined (reflected along same axis) and passed through optics to display



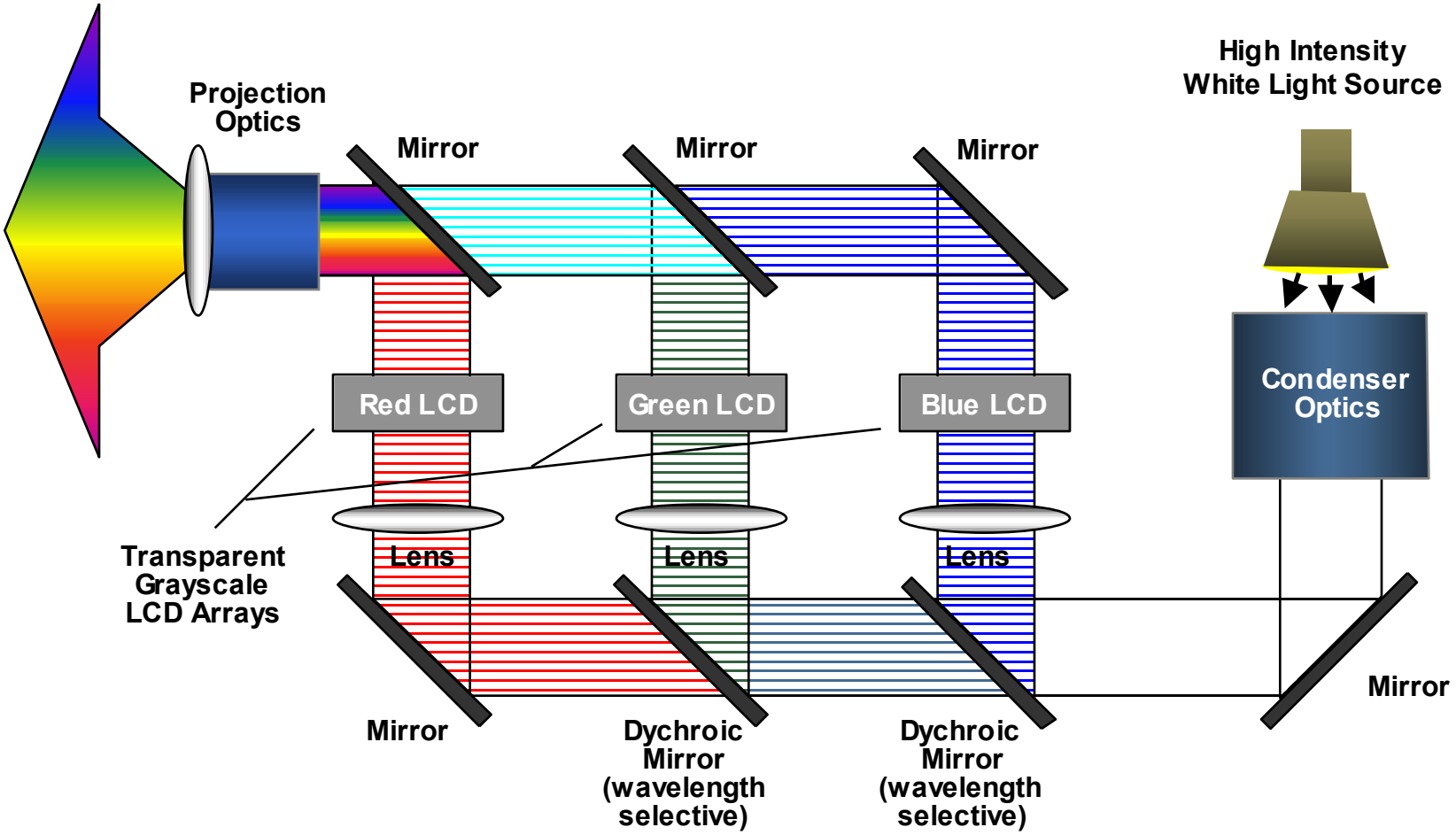
Courtesy of: Texas Instruments

- Reduced mechanics (no spinning wheel) means the system is more reliable
- Dedicated mirrors also mean higher quality pictures

LCD Sub-pixel Structure Cross Sectional View

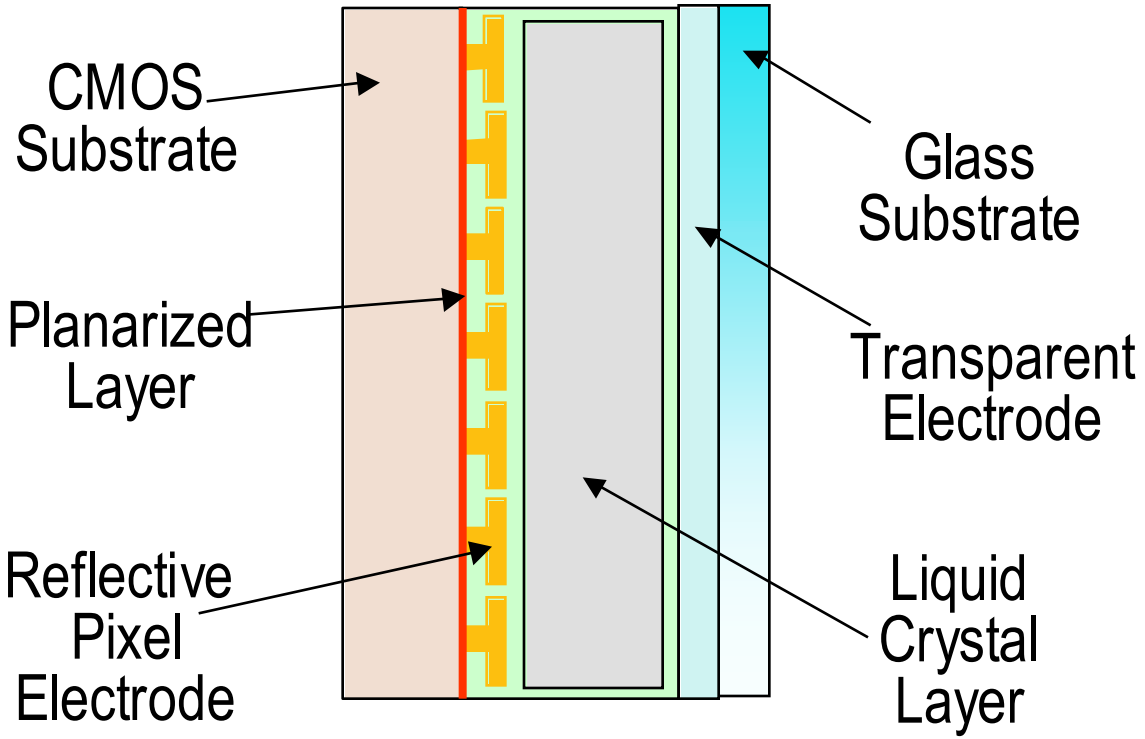


LCD Projection



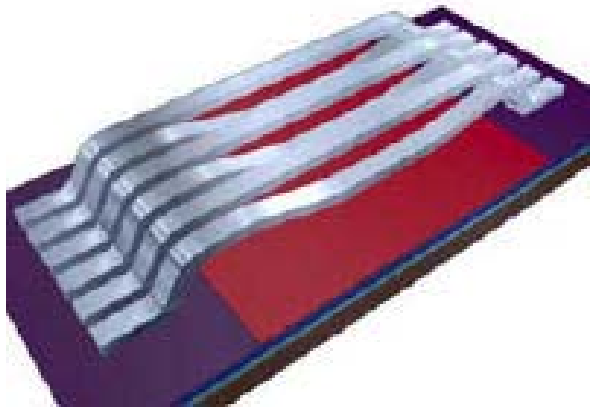
JVC D-ILA LCOS Technology

Cross Sectional View



Grating Light Valve (GLV)

- Developed at Stanford University and manufactured by Silicon Light Image
- Each ribbon can be moved towards the chip by a fraction of the wavelength of light forming a diffraction grating pattern and therefore pixel information
- A vertical linear array of 1,080 of these GLV pixels is constructed
- Red, green and blue lasers are then directed at the linear array and the light output is rapidly scanned across the display screen

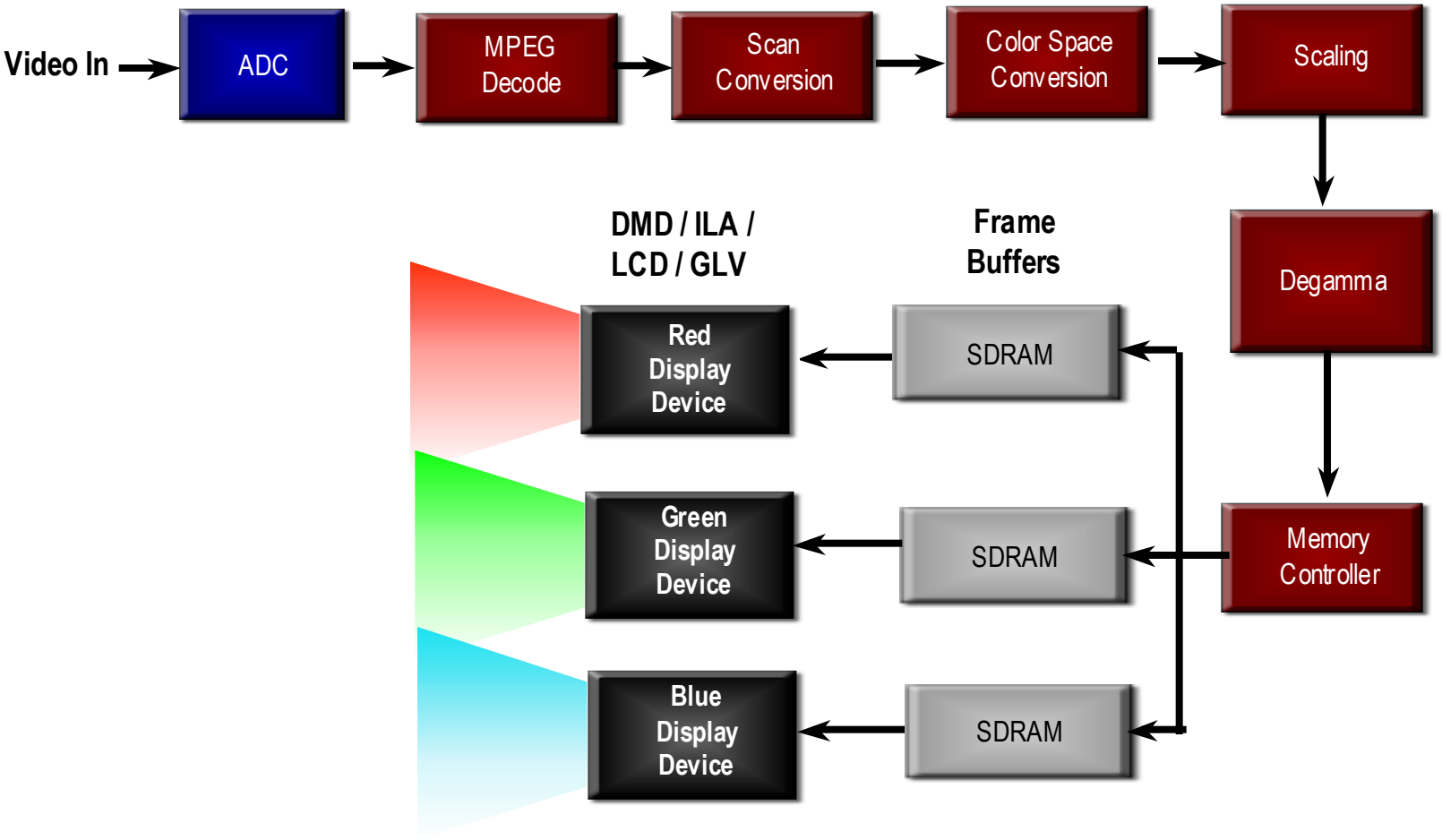


Courtesy: Silicon Light Image

D-Cinema Standards

- Efforts from various bodies to ensure interoperability while retaining competitiveness
  - Society of Motion Picture and Television Engineers (SMPTE)
  - Motion Pictures Association (MPAA)
  - Moving Pictures Experts Group (MPEG)
  - Entertainment Technology Center (ETC)
- Still concerns in the industry that standards still allow confusion and interoperability uncertainties
  - Re-programmable FPGA solutions would remove some of these concerns
- Standards from existing technologies may need to be used to keep costs down (e.g. TDES Encryption)

Digital Cinema Projector System



Digital | Memory | Mixed Signal | *uP or uC* | Programmable | *IP Block*

XILINX®

Problems Facing D-Cinema

- Different experience from theatre to theatre (or home to home)
  - Ambient light, display/screen reflectivity, projector lamp intensity and optics
  - Can consumers/theatre owners understand requirements for optimal presentations?
- Not enough standardization
  - SMPTE DC28 trying to solve this but currently no OEM products really support DC28 for real-time applications
  - Interoperability between display types (e.g. DLP and ILA) still to be addressed
    - New color gamut standard required?
- Huge storage and bandwidth requirements
  - Up to 200 terabytes per film during post production stage
- Digital content protection and rights management
  - Cryptography paramount to combat pirating

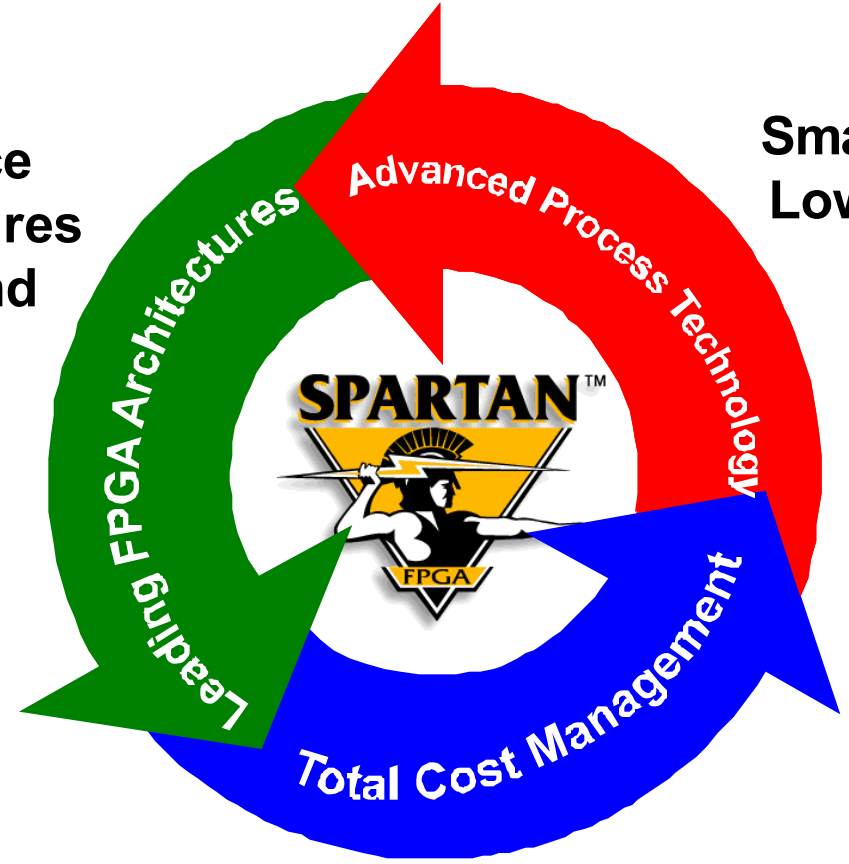
Xilinx Solutions for D-Cinema

- Projectors with programmable settings for adaptation to environment
  - Digital adjustments and DSP techniques to make up for poor optics, and different light levels
  - On-line reprogrammability to transfer technology -understanding burden from the customer back to the equipment manufacturer
- Programmable solutions to new standard adoption/variation
  - Faster time-to-market + longer time-in-market = $$$ for manufacturer
  - Programmable adaptation to different input formats or output display types
  - Parameterizable color spaces available now rather than waiting for an ASSP solution
- Programmable cryptography for new algorithms should existing ones be compromised

Introducing the Spartan-IIE FPGA Family

Xilinx Spartan Series FPGAs

High Performance System Features Software and Cores



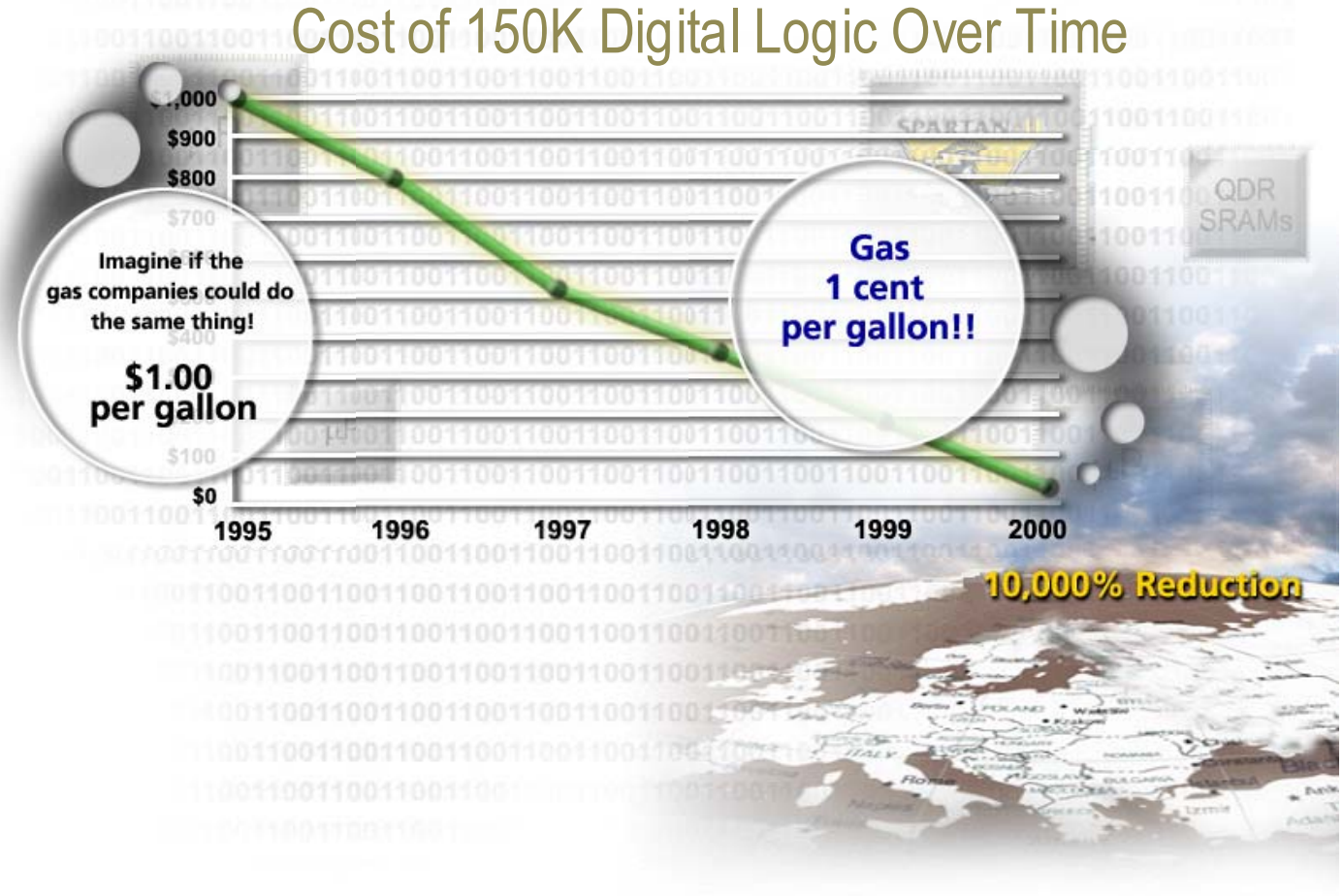
Smallest Die Size Lowest Possible Cost

Low Cost Plastic Packages Streamlined Testing

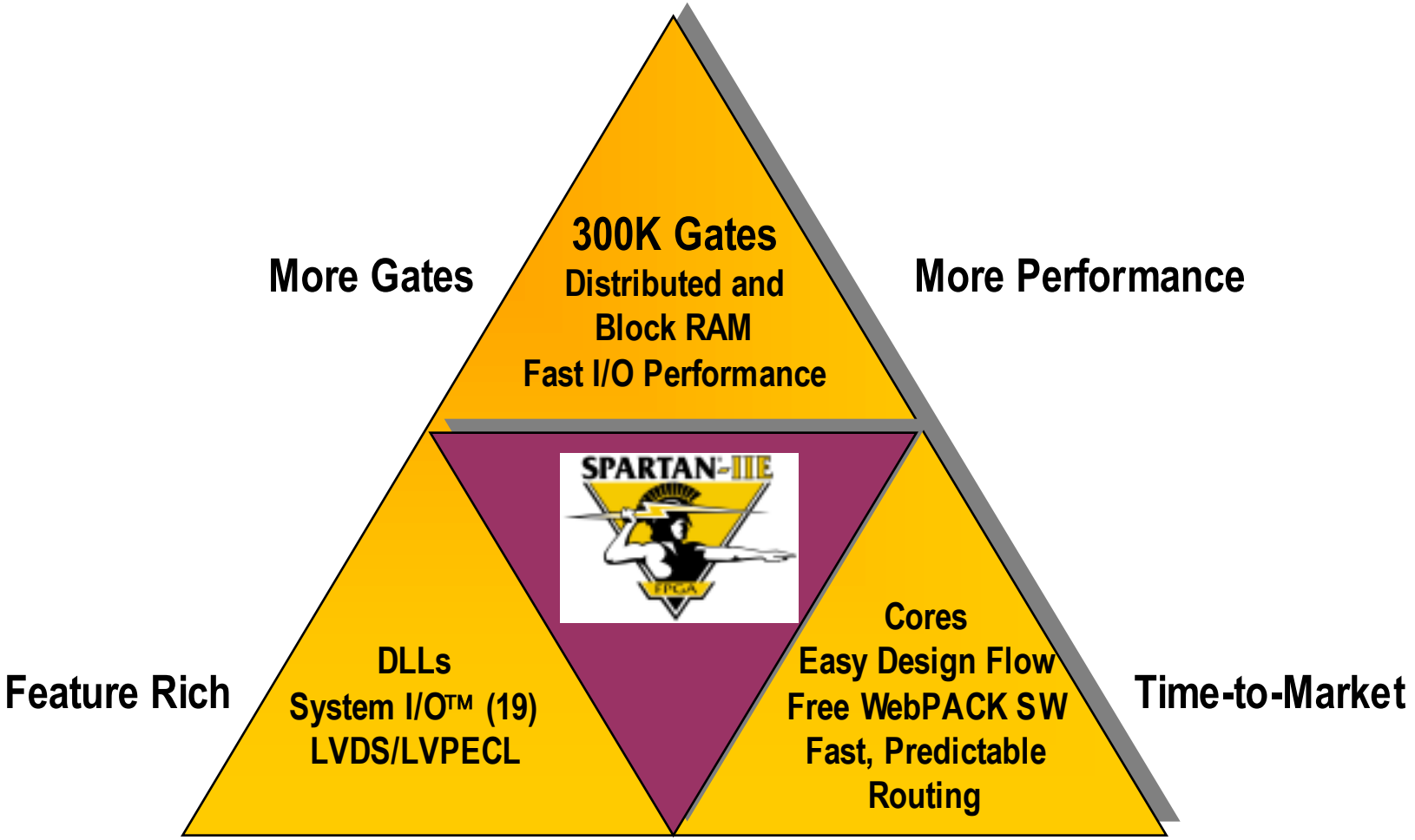
Spartan-IIE FPGAs
A Natural Fit for Digital Convergence

- Xilinx Solutions Allow Customers To Thrive in Chaos
  - FPGAs traditionally offer fast time-to-market
    - First to market, increases market share and revenue advantage
  - Xilinx Online offers re-configurability in the field
    - Allows shipped product to support revisions to the spec
    - Enables unique opportunities to add value
    - Increases lifecycle revenue yield and hence, time-in-market
  - Enables rapid product proliferation
    - New designs can be quickly turned into derivatives
  - Superior lifecycle component logistics
  - Proven FPGA technology, software, and test benches
- Spartan-IIE FPGAs Are Cost Effective!!!

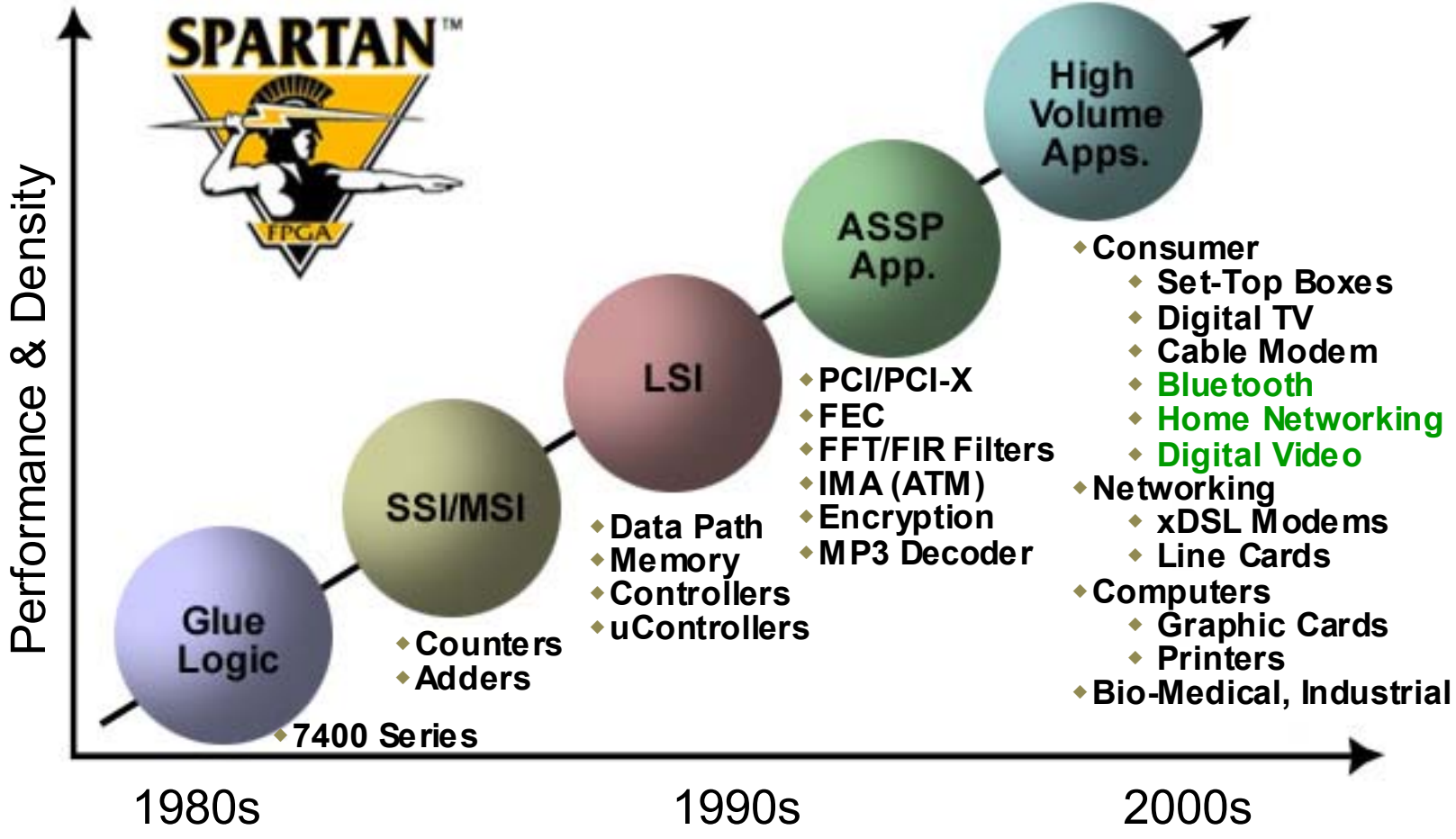
Taking the Cost Down...



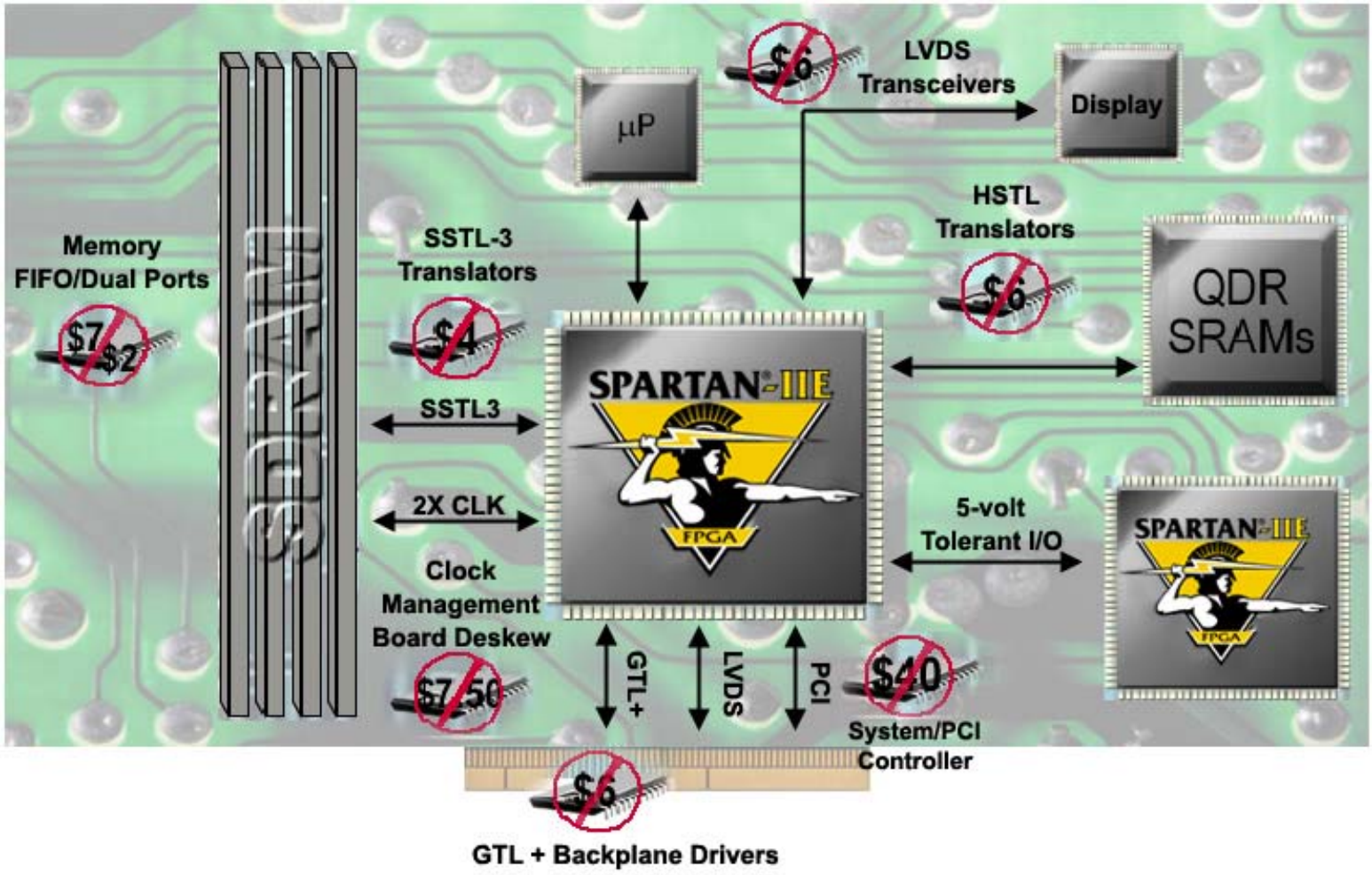
Spartan-IIE: The Total Solution



FPGA Application Trends



Spartan-IIE - System Integration



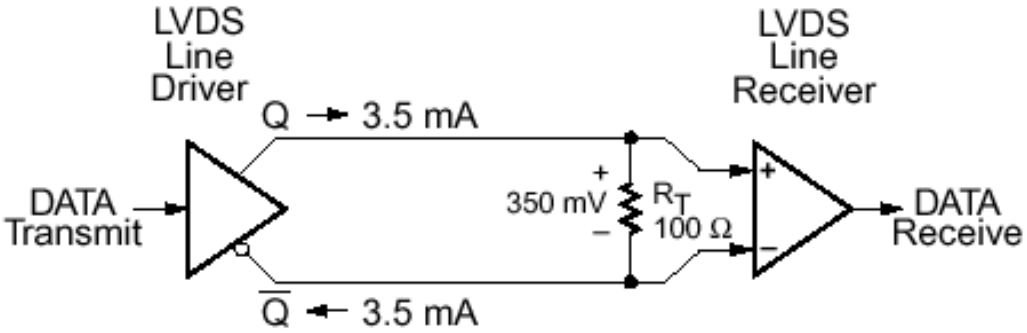
Spartan-IIE Features
Value for Digital Video

Spartan-IIE Silicon Features	Value for Digital Video Applications
FPGA Fabric and Routing, Up to 300,000 System Gates	Performance in excess of 20 billion MACs/second
Delay Locked Loops (DLLs)	Clock multiplication and division, clock mirror, Improve I/O Perf.
SelectIO - HSTL-I, -III, -IV	High-speed SRAM interface
SelectIO - SSTL3-I, -II; SSTL2-I, -II	High-speed DRAM interface
SelectIO - GTL, PCI, AGP	Chip-to-Backplane, Chip-to-Chip interfaces
Differential Signaling - LVDS, Bus LVDS, LVPECL	Bandwidth management (saving the number of pins), reduced power consumption, reduced EMI, high noise immunity
SRL-16	16-bit Shift Register ideal for capturing high-speed or burst-mode data and to store data in DSP applications
Distributed RAM	DSP Coefficients, Small FIFOs
Block RAM	Video Line Buffers, Cache Tag Memory, Scratch-pad Memory, Packet Buffers, Large FIFOs

What is LVDS?

- LVDS - Low Voltage Differential Signaling
- LVDS is a differential signaling interconnect technology
  - Requires two pins per channel
- LVDS was first used as a interconnectivity technology in laptops and displays to alleviate EMI issues
- Technology is now widely used
  - A broad spectrum of telecom and networking applications
  - Mainstream consumer applications like digital video and displays

LVDS Technology

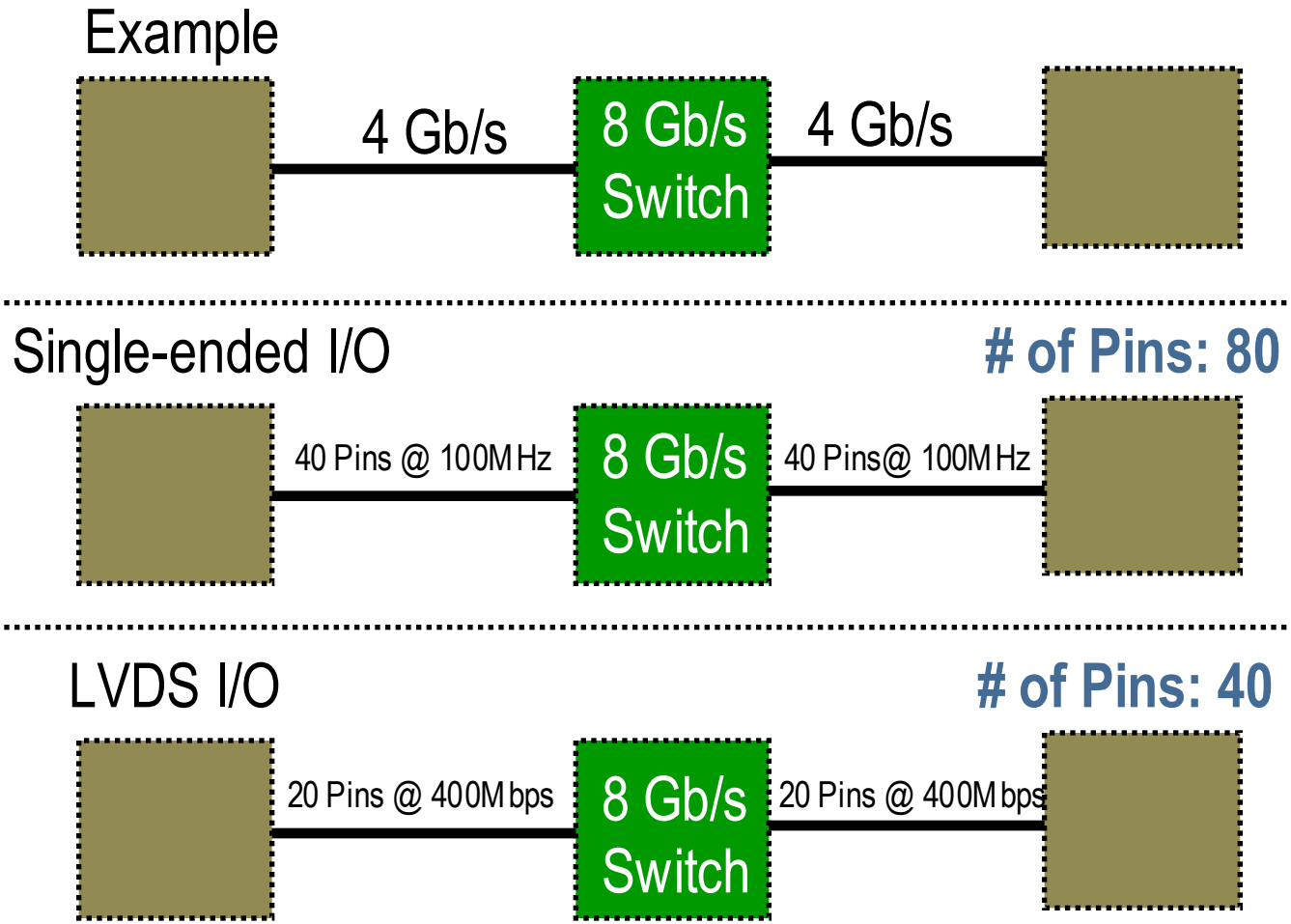


DC Parameter	Conditions	MIN	TYP	MAX	Units
Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	-	1.38	1.6	V
Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.90	1.03	-	V
Differential Output Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	250	350	450	mV
Output Common-Mode Voltage (Q + $\overline{Q}$) / 2	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.25	1.375	V
Differential Input Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25 V	100	350	-	mV
Input Common-Mode Voltage (Q + $\overline{Q}$) / 2	Differential input voltage = ±350 mV	0.25	1.25	2.25	V

Differential Signaling Benefits

- Higher performance per pin pair
- Reduced EMI
  - Low output voltage swing
  - Relatively slow edge rates (dV/dt)
- High noise immunity
  - Switching noise cancels between the two lines
  - Data is not affected by the noise
    - External noise affects both lines, but the voltage difference stays about the same
- Reduced Power Consumption

LVDS Benefits - Save # of Pins



LVDS - Xilinx Support

LVDS Use Model	Spartan-IIE		Virtex-II	
	Support	Mbps/Channel	Support	Mbps/Channel
System Applications	Yes	400	Yes	840
Networking & Telecom	Yes	400	Yes	840
High-End Display Driver	No	N/A	Yes	840

Spartan-IIE Differential I/O Counts

	TQ144		PQ208		FT256		FG456	
Device	User	Diff	User	Diff	User	Diff	User	Diff
XC2S50E	102	28	146	50	182	84		
XC2S100E	102	28	146	50	182	84	202	86
XC2S150E			146	50	182	84	263	114
XC2S200E			146	50	182	84	289	120
XC2S300E			146	50	182	84	329	120

User = Maximum number of User I/Os available
Diff = Maximum number of Differential Paired I/Os available

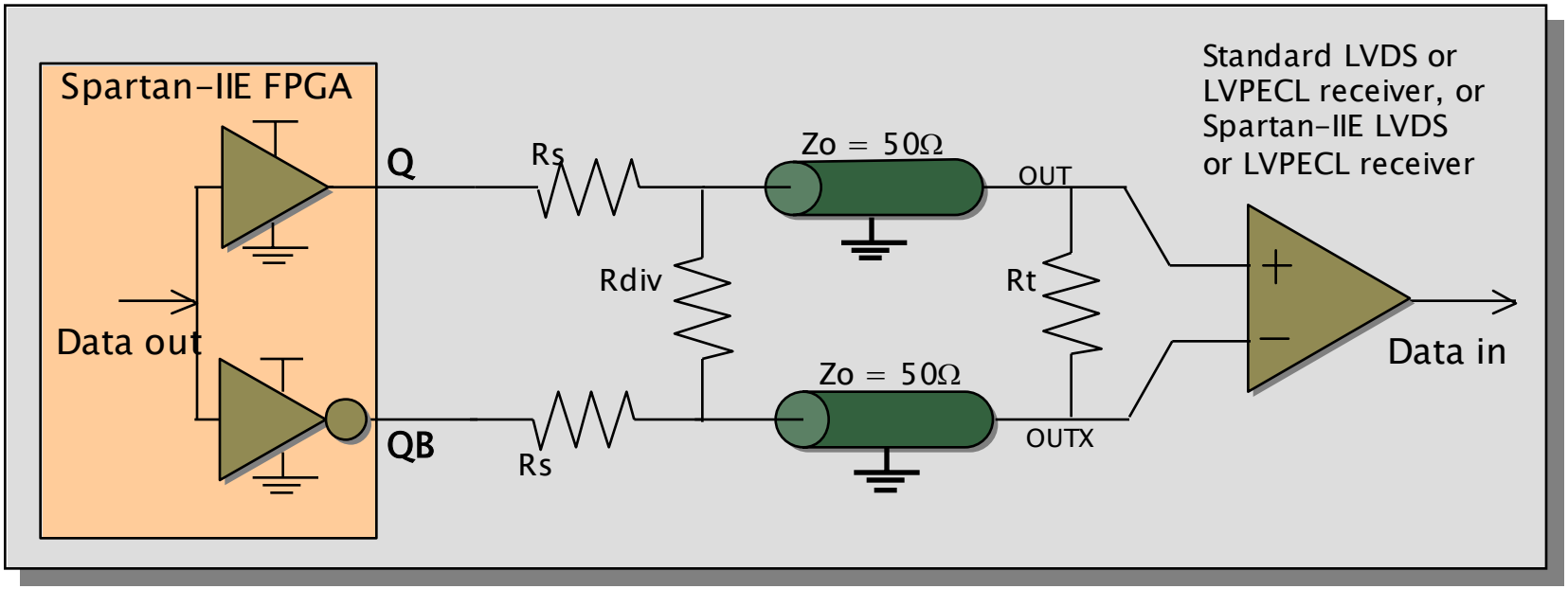
Spartan-IIE LVDS Support

- All IOBs have LVDS/BLVDS/LVPECL capability
- IOBs configured as LVDS can be:
  - Synchronous or asynchronous
  - Input or output
- Two IOBs (pair) form one LVDS signal
  - One IOB will function as + or P
  - The other IOB will function as - or N
- LVDS pin pairs are indicated in the datasheet
- Maximum number of LVDS pin-pairs = 120

Bus LVDS and LVPECL

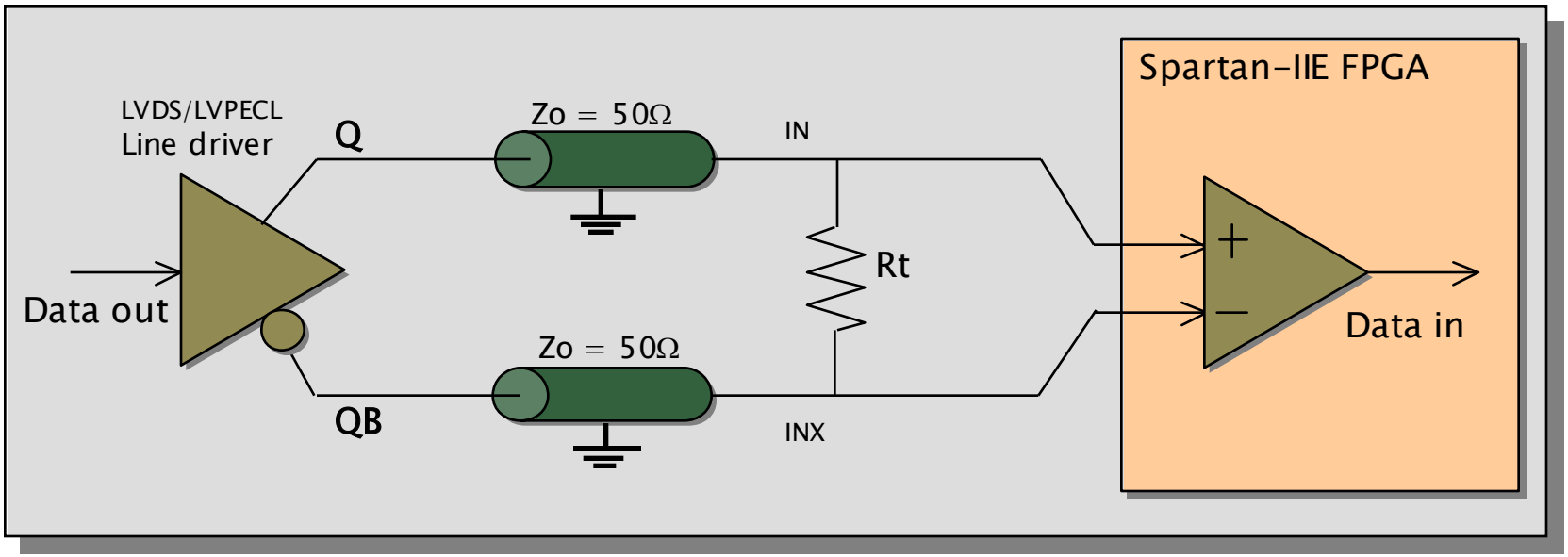
- Bus LVDS - Bi-directional LVDS
  - The device can transmit and receive LVDS signals through the same pins
  - Requires different termination than LVDS
- LVPECL - Low Voltage Positive Emitter Coupled Logic
  - Well known industry standard for fast clocking and interconnectivity
  - Voltage swing (~750 mV) over two differential connections

Spartan-IIE as a Differential Driver



Capable of driving any standard LVDS or LVPECL receiver

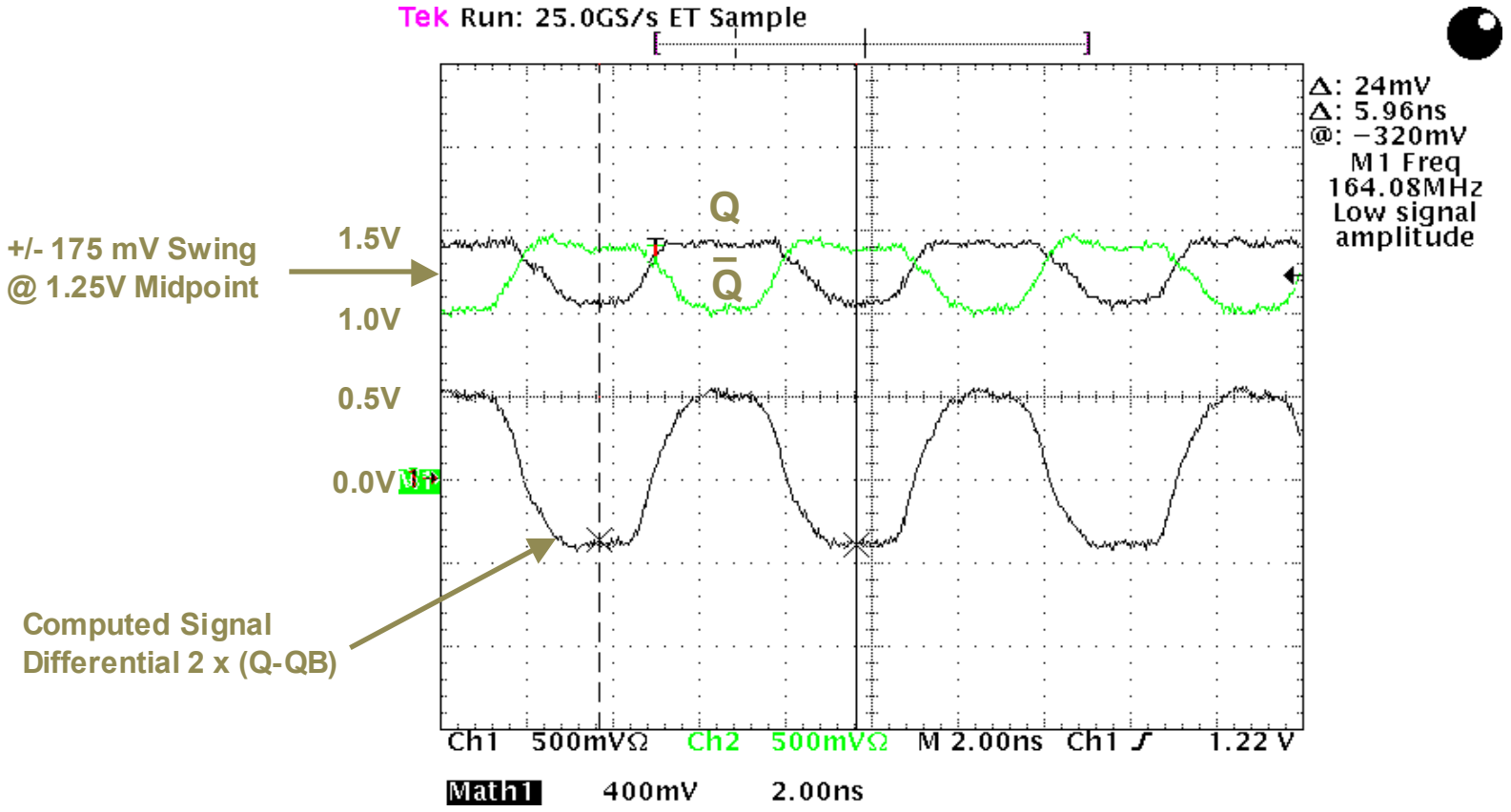
Spartan-IIE as a Differential Receiver



Spartan-IIE can be driven by any standard LVDS or LVPECL driver

Spartan-IIE receiver complies with the LVDS or LVPECL specs

Spartan-IIE LVDS Signaling



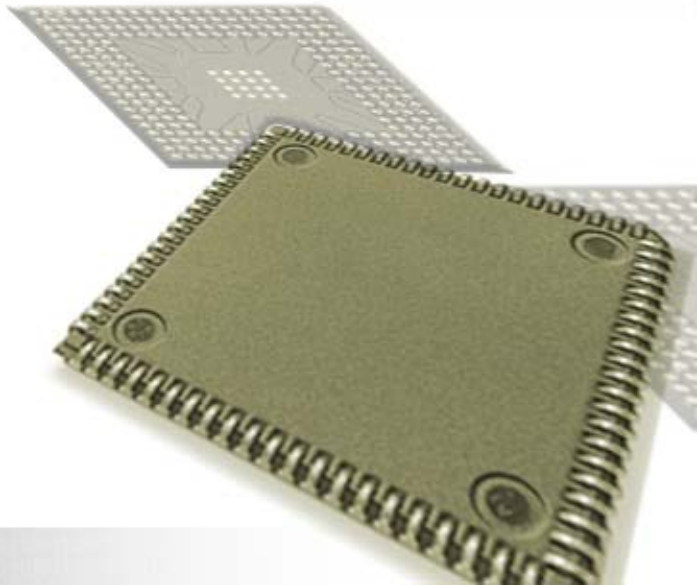
Spartan-IIE Core Support

- On-chip memory & storage
  - Distributed, BlockRAM, FIFOs
- Bus products
  - PCI (64- & 32-bit, 33/66MHz), Arbiter, CAN bus interface
- DSP functions (FIR filter)
- Error correction
  - Reed-Solomon, Viterbi
- Encryption (DES & triple DES)
- Microprocessor
  - ARC 32-bit configurable RISC, 8-bit 8051 microcontroller
- Memory controllers (10+)
  - SDRAM, QDR SRAM
- Communications
  - ATM (IMA, UTOPIA), Fast Ethernet (MAC)
- Telecom
  - CDMA matched filter, HDLC, DVB satellite, ADPCM speech codec
- Video & image processing
  - JPEG codec, DCT/IDCT, color space converter
- UARTs

Programmable Color Space Conversion

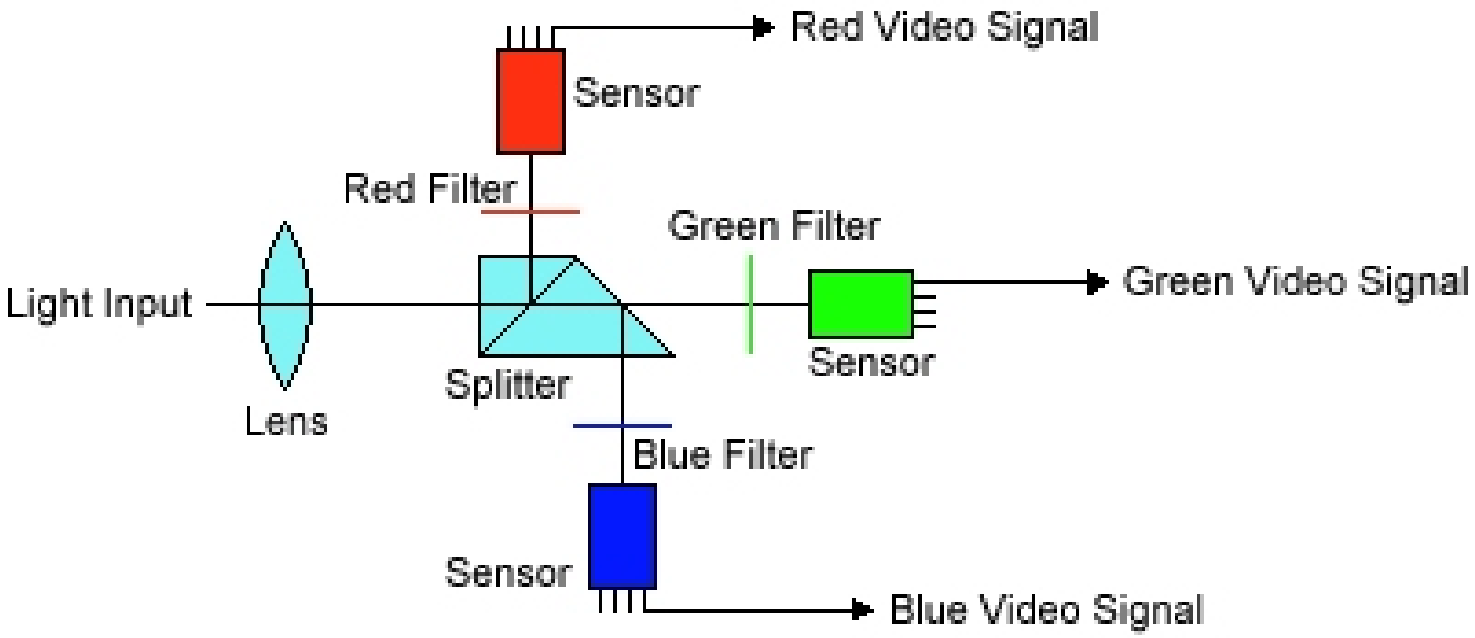
"The mission of Xilinx is to help our customers attain the fastest time-to-market and flexible product life cycle management through programmable logic solutions consisting of software, silicon and support."

Wim Roelandts
President and CEO



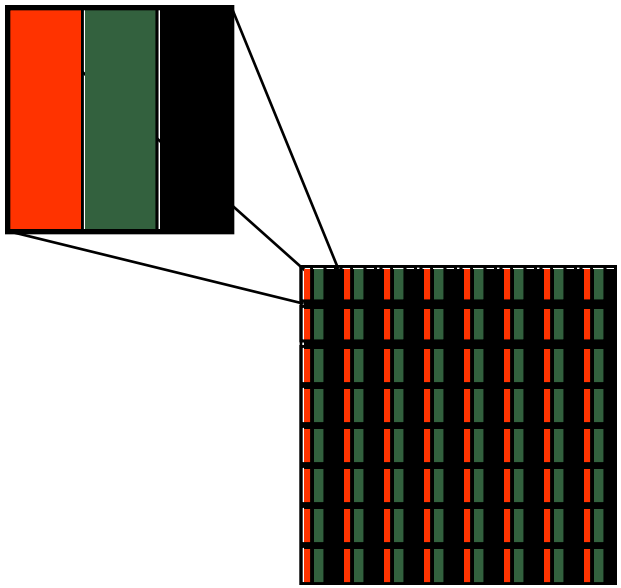
Basic Camera System

A camera basically splits the incoming light source into three electrical color components : red, green and blue

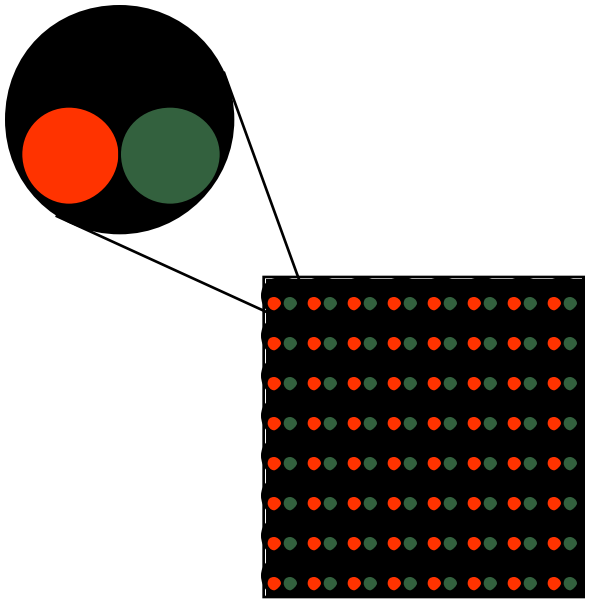


Anatomy of a Pixel

- At the display, pixels are comprised of red, green and blue color producing elements



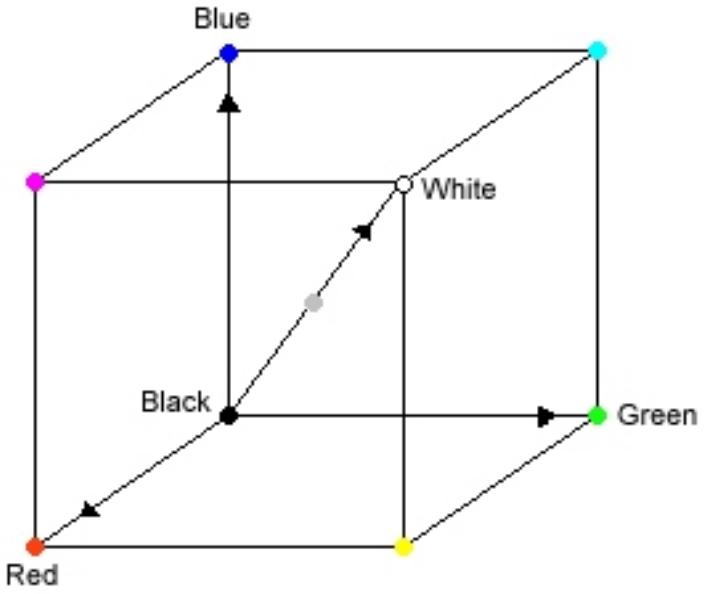
LCD



CRT

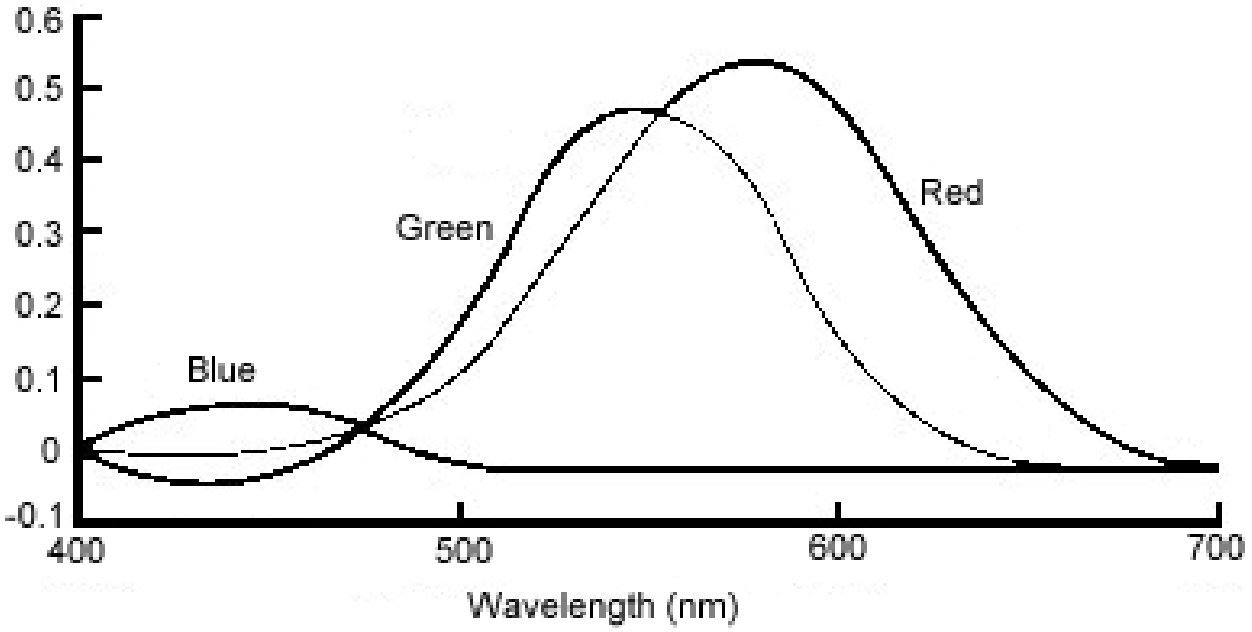
RGB Unity Color Space

Mixtures of color components can be mapped into an RGB color space covering all variations from black (0xR + 0xG + 0xB) to white (1xR + 1xG + 1xB)



Spectral Response of Human Eye

Green sensing cones in the human eye respond to most wavelengths in the light spectrum

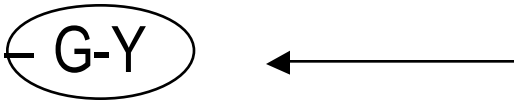


Luminance and Color Difference

- Pictures are almost always represented as pixels on final medium
  - Whether it be printed paper or TFT, PDP & CRT displays
- Pixels can be represented with 3 full bandwidth analog RGB components
  - Huge storage and transmission bandwidth requirements for high resolution, large format displays (up to 200 terabytes during post production)
- Human eye is more receptive to brightness than it is to color
  - Full resolution of human vision is restricted to brightness variations
  - Color detail resolution is about a quarter that of brightness variations
  - Green objects will produce more stimulus than red objects of the same brightness, with blue objects producing the least
- A brightness/luma signal (Y) can be obtained by adding RGB values together which are weighted by relative eye response

Luminance and Color Difference

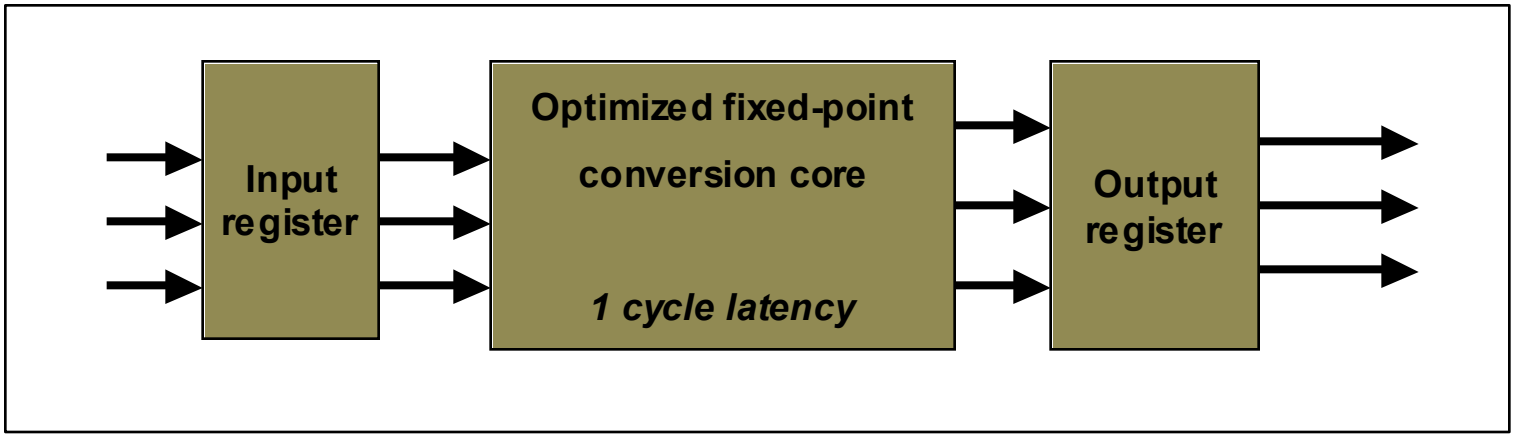
- ITU CCR 601 says Y = 0.299R + 0.587G + 0.114B
- To save bandwidth, color difference signals sent with luma rather than RGB
- Color difference possibilities
  - R-Y
  - B-Y
  - G-Y



As G contributes most to Y, this signal would be small and most susceptible to noise

- Simple math can be used to reconstruct signals at the display

Color Space Converter Structure



- Fully synchronous
- Registered input and output, 1 internal pipeline stage
  - Low latency (3 cycles)
- Continuous processing
  - One 3-color conversion every clock cycle
- Internal 10-bit precision for accuracy
  - Rounded to 8-bit outputs\

Xilinx Cores Available

CCIR 601 Standard

- RGB2YCrCb
- Y = 0.257×R' + 0.504×G' + 0.098×B' + 16
- Cr = 0.439×R' - 0.368×G' - 0.071×B' + 128
- Cb = -0.148×R' - 0.291×G' + 0.439×B' + 128
- YCrCb2RGB
- R'= 1.164×(Y-16) + 1.596×(Cr-128)
- G' = 1.164×(Y-16) - 0.813×(Cr-128) - 0.392×(Cb-128)
- B' = 1.164×(Y-16) + 2.017×(Cb-128)
- RGB2YUV
- Y = 0.299×R' + 0.587×G' + 0.114×B'
- U = -0.147×R' - 0.289×G' + 0.436×B'
- V = 0.615×R' - 0.515×G' - 0.100×B'
- YUV2RGB
- R' = Y + 1.140×V
- G' = Y - 0.394×U - 0.581×V
- B' = Y - 2.032×U

R'G'B' refers to gamma corrected RGB

Color Space Converter Lounge
www.xilinx.com/ipcenter

Memory Controllers

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logic solutions consisting of
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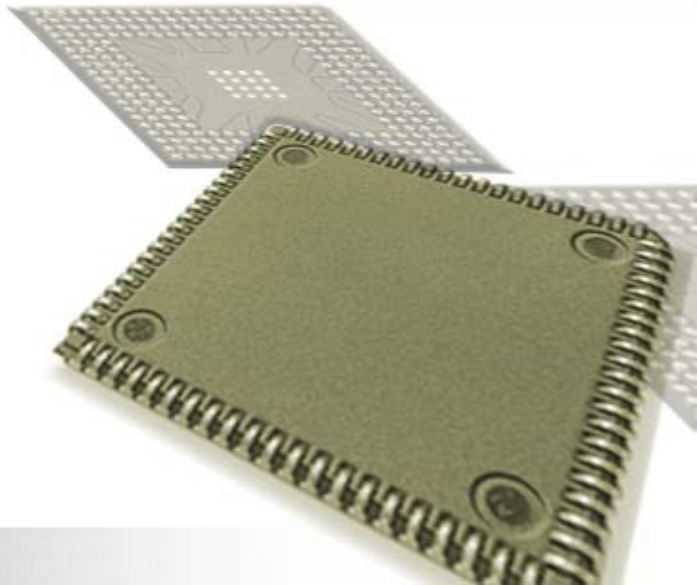
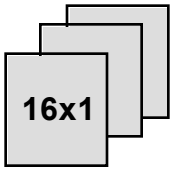
Wim Roelandts
President and CEO



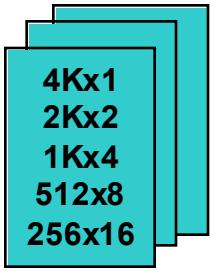
Spartan-IIE Memory Solutions

Distributed RAM



DSP Coefficients
Small FIFOs

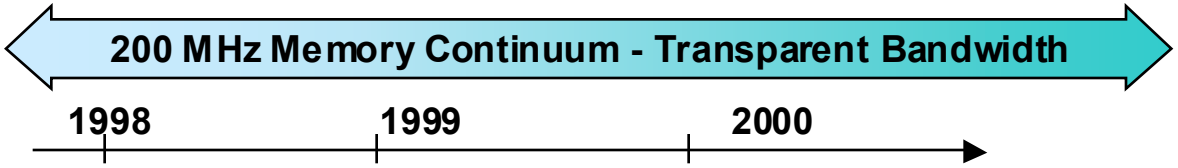
Block RAM



Large FIFOs
Video Line Buffers
Cache Tag Memory

External Memory Interface

SDRAM
SGRAM
PB SRAM
DDR SRAM
ZBT SRAM
QDR SRAM

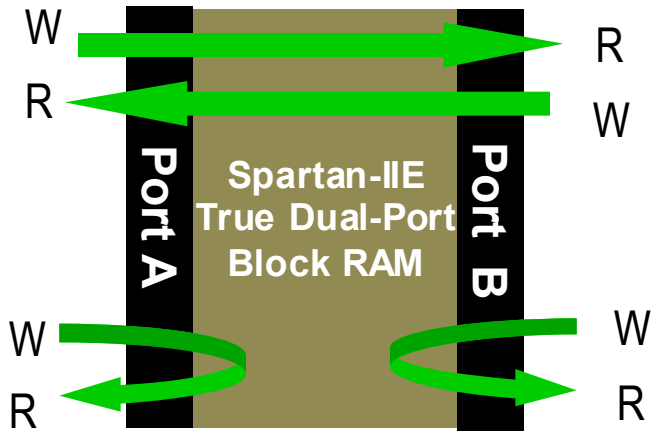


Spartan-IIE Core Support

- On-chip memory & storage
  - Distributed, BlockRAM, FIFOs
- Bus products
  - PCI (64- & 32-bit, 33/66MHz), Arbiter, CAN bus interface
- DSP functions (FIR filter)
- Error correction
  - Reed-Solomon, Viterbi
- Encryption (DES & triple DES)
- Microprocessor
  - ARC 32-bit configurable RISC, 8-bit 8051 microcontroller
- Memory controllers (10+)
  - SDRAM, QDR SRAM
- Communications
  - ATM (IMA, UTOPIA), Fast Ethernet (MAC)
- Telecom
  - CDMA matched filter, HDLC, DVB satellite, ADPCM speech codec
- Video & image processing
  - JPEG codec, DCT/IDCT, color space converter
- UARTs

Spartan-IIE Block RAM

- True Dual-port Static RAM - 4K bits
  - Independently configurable port data width
    - 4K x 1; 2K x 2; 1K x 4; 512 x 8; 256 x 16
  - Fast synchronous read and write
    - 2.5-ns clock-to-output with 1-ns input address/data setup



Data Flow	Spartan-IIE
A to B	Yes
B to A	Yes
A to A	Yes
B to B	Yes

Spartan-IIE Memory Controllers

- Spartan-IIE FPGAs
  - Unique and extensive features, flexible architecture, low cost
- Memory controller for interface to different types of SRAM, DRAM & Flash memory
  - Xilinx provides FREE VHDL source code for implementing the memory controllers in Spartan-IIE

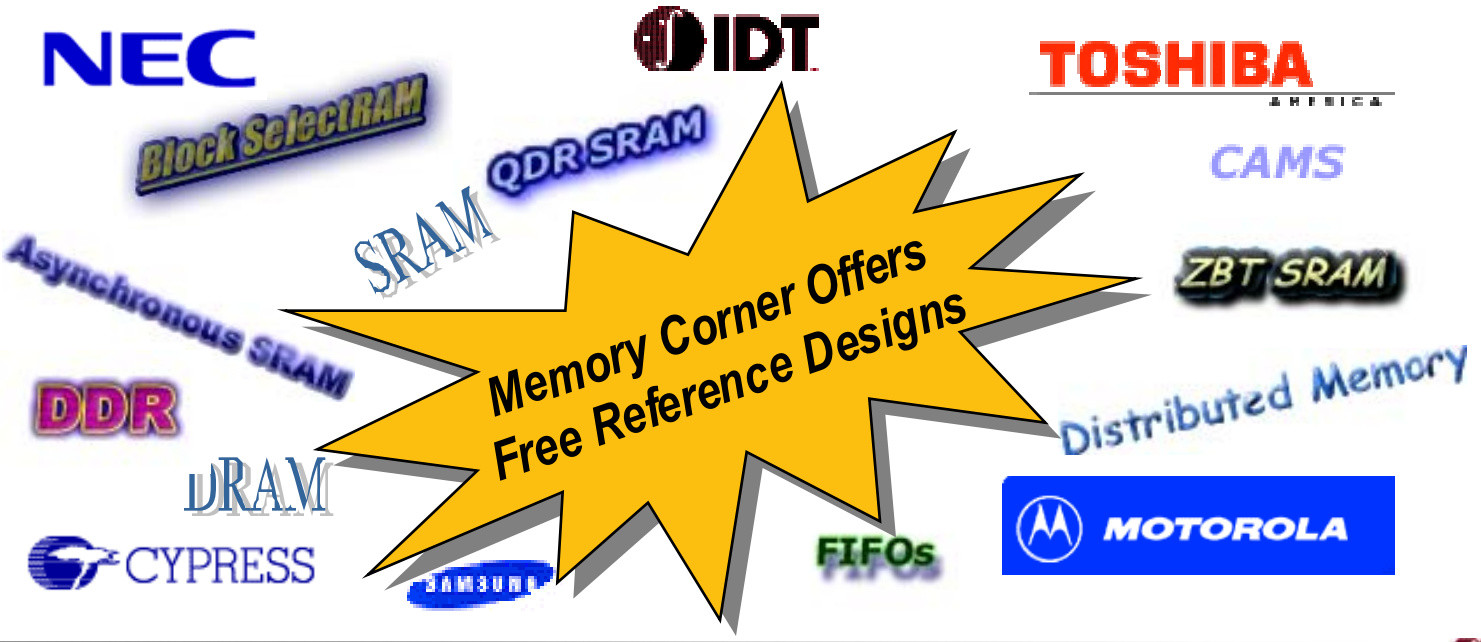
Memory Controller Reference Designs

- DRAM reference designs
  - 64-bit DDR DRAM controller
  - 16-bit DDR DRAM controller
  - SDRAM controller
- SRAM reference designs
  - ZBT SRAM controller
  - QDR SRAM controller
- Flash controller
  - NOR / NAND flash controller
- Embedded memory reference designs
  - CAM for ATM applications
  - CAM using shift registers
  - CAM using Block SelectRAM
  - Data-width conversion FIFO
  - 170MHz FIFO for Virtex
  - High speed FIFO for Spartan-IIE

These Reference Designs are Available for Immediate Download at the Memory Corner

Memory Corner

- Collaboration between Xilinx and major memory vendors to provide comprehensive web-based memory solutions
  - Free reference designs (VHDL/Verilog)
  - SRAM, DRAM & embedded FPGA memory solutions
  - Data sheets, app notes, tutorials, FAQs, design guidelines



Data Encryption

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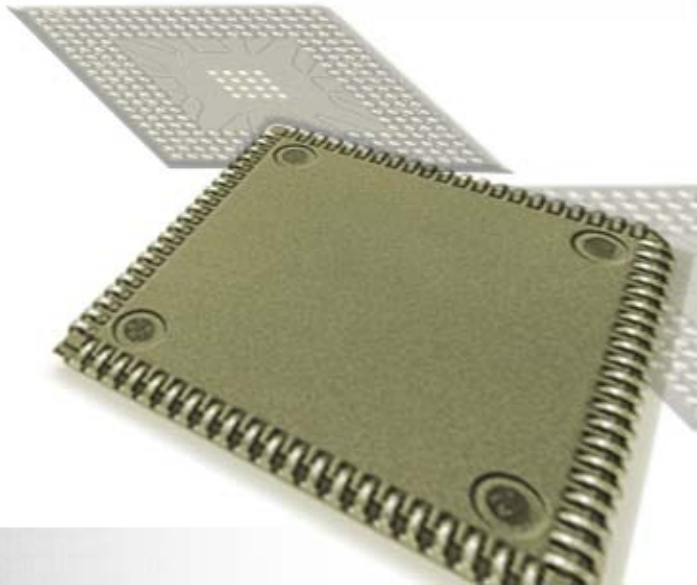


Copy Protection and Data Encryption

- Motivation for data encryption & cryptography
  - Data privacy (Integrity & Secrecy)
  - Authenticating the source of the information
- Several methods of data encryption exist
  - RSA (Rivest-Shamir-Adleman), Diffie-Hellman, RC4/RC5
  - Secure Hashing Algorithm (SHA), Blowfish
  - Elliptic Curves, ElGamal, LUC (Lucas Sequence)
  - DES (Data Encryption Standard) & Triple-DES (TDES)
- Xilinx Spartan-IIE + IP Cores today provide
  - AES, DES, Triple DES, proprietary

Copy Protection Efforts

Copy-protection efforts at a glance

- CPTWG (a cross-industry forum among the movie, PC and consumer electronics industries): Five-year-old group meets regularly to propose and discuss technology issues related to DVD, including copy protection, encryption and watermarking.

- 5C (formed by Intel Corp., Hitachi Ltd., Sony Corp, Toshiba Corp. and Matsushita Electric Industrial Co.): Worked to develop Digital Transmission Content Protection (DTCP) to define a cryptographic protocol copy protection.

- 4C (initiated by Intel, IBM, Matsushita and Toshiba): Working on a Content Protection for Recordable Media and Pre-Recorded Media (CPRM/CPPM) specification that defines a renewable cryptographic method to protect entertainment content recorded on physical media.

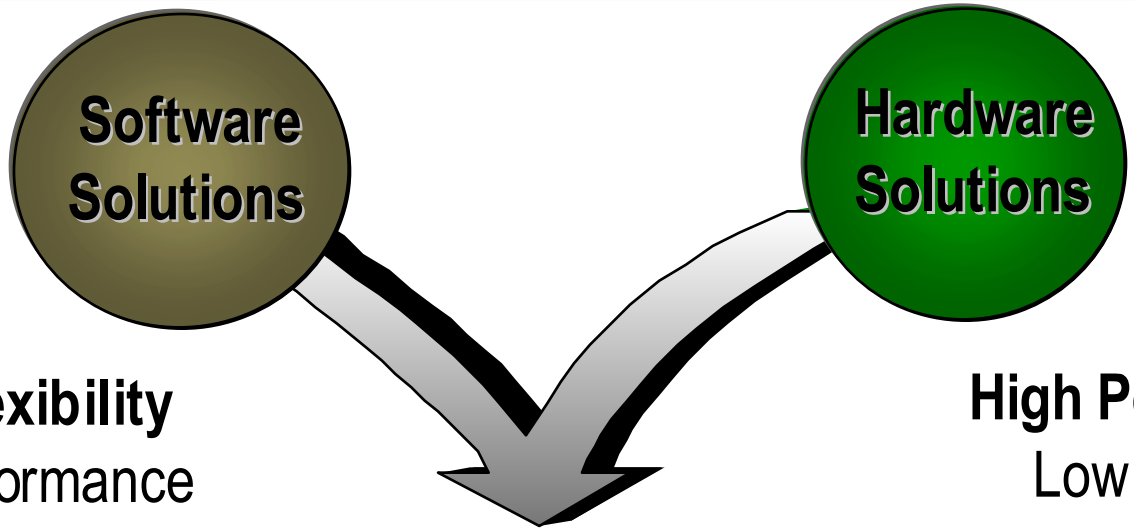
- TCPA (formed by Compaq, HP, IBM, Intel and Microsoft): Focuses on developing a specification to deliver a set of hardware and operating-system security capabilities that customers can use to "enhance the trust and security in their computing environments," the group said.

Courtesy: EETimes

Copy Protection
FPGAs Add Significant Value

- Security Systems Standards and Certification Act (Draft)
  - Calls for interactive digital devices to include security technologies certified by the U.S. Secretary of Commerce
- The bill becoming a law will prevent companies from shipping products without appropriate security
  - There is however no guidance on security schemes
  - A hardware based security implementation is preferred
- Lack of consensus between companies on the encryption schemes and their implementation is leading to chaos
- Copy protection for digital video products is in it's infancy and will be a significant area of focus

Spartan-IIE Advantages Over Hardware & Software Solutions



High Flexibility
Low Performance

High Performance
Low Flexibility

High Performance
High Flexibility

Enhanced Security & Performance

DES Concept

- The Data Encryption Standard (DES) algorithm
  - Developed by IBM Corporation
  - Most prevalent encryption algorithm
  - Adopted by the U.S. government in 1977, as the federal standard for encryption of commercial and sensitive, yet unclassified data
  - Is a block cipher
    - Encryption algorithm that encrypts block of data all at once, and then goes on to the next block
  - Divides 64-bit plaintext into blocks of fixed length (ciphertext)
  - Enciphers using a 56-bit secret internal key

Triple-DES Concept

- Triple-DES concept
  - More powerful & more secure
  - Equivalent to performing DES 3 times on plaintext with 3 different keys
  - TDES use 2 or 3 56-bit keys
  - With one key, TDES performs the same as DES
  - TDES implementation: serial and parallel
    - Parallel improves performance and reduces gate count

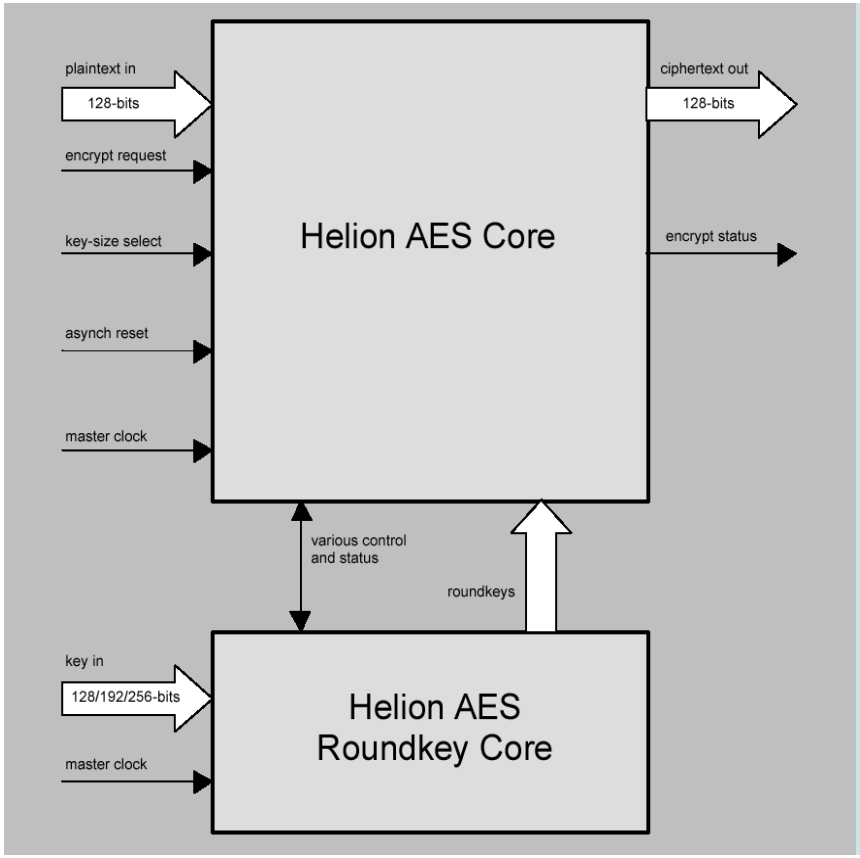
Value Proposition
DES and Triple DES

- High performance, many features and cost effective
- High scalability and flexibility
  - Reconfigurable fabric and Internet Reconfigurable Logic
- Embedded solutions
  - FPGA logic not used from DES/Triple-DES soft IP can be used for other IP solutions
    - DCT/IDCT and DES/TDES soft IP in a Spartan-IIE FPGA can be used in multimedia and imaging applications
  - Increase the value proposition and reduces solution cost
- Spartan-IIE can be programmed with broadcaster proprietary conditional access algorithms

AES (Rijndael)

- AES (Rijndael) chosen by the National Institute of Standards and Technology (NIST) as the cryptographic algorithm for use by U.S. government organizations to protect sensitive (unclassified) information
  - Rijndael block cipher named after its Dutch developers Vincent Rijmen and Joan Daemen
- Aimed to replace DES over long term
  - DES has been successfully attacked using dedicated hardware and parallel computer networks
  - DES to be phased out
- Triple-DES expected to remain for foreseeable future

AES (Rijndael)
IP Solutions - Helion Technology



Features

- Implements AES (Rijndael) to latest NIST FIPS proposal
- 128-bit block-size, option of 128, 192 or 256-bit key-size (can be changed dynamically)
- Very fast operation – completes one AES round per master clock
- Supports data rates in excess of 10Gbps
- Separate encrypt and decrypt cores available
- Supports optional real-time roundkey generation
- All AES operating modes easily implemented (eg. ECB, CBC, OFB, CFB, MAC)
- Simple external interface
- Highly optimised for use in Xilinx FPGA technologies

Deliverables

- Target specific netlist or fully synthesisable RTL VHDL
- VHDL simulation model and testbench with FIPS test vectors
- User documentation

HELION

XILINX®

Spartan-IIE Encryption Solutions

- Spartan-IIE encryption solutions are NIST approved
- The programmable nature of these solutions allows easy customization based on the end application requirement

	Spartan-IIE Solution			
	DES	Triple-DES	AES	AES
Device	2S100E-6	2S150E-6	2S100E-6	2S100E-6
CLB Slices	235	1611	358*	231**
Performance	94 MHz	48 MHz	82 MHz	82 MHz
Area Utilization	19.58%	93.22%	29.83%	19.25%
Key Size	56-bit	128-bit or two 64-bit	128/192/ 256-bit	128/192/ 256-bit

Note: Solution includes encryption, decryption and key generation

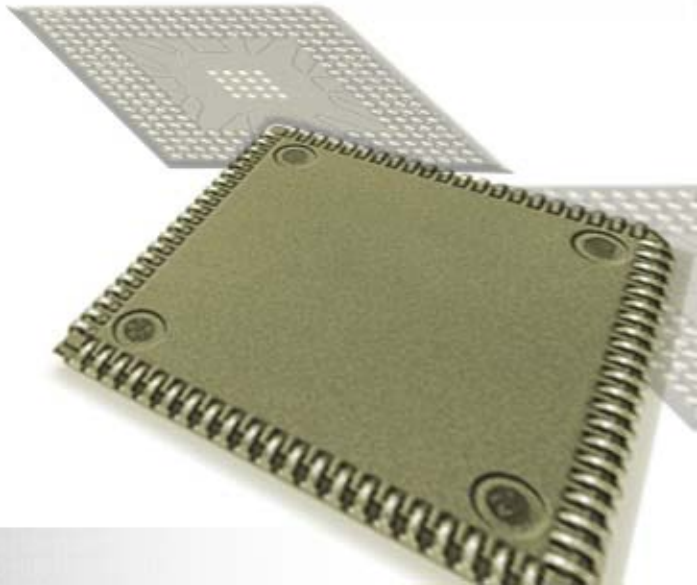
* 128-bit key implementation

** Key Generation offloaded to embedded µC/ µP

Clock Generation & Distribution

"The mission of Xilinx is to help our customers attain the fastest time-to-market and flexible product life cycle management through programmable logic solutions consisting of software, silicon and support."

Wim Roelandts
President and CEO



Clock Generation and Distribution

- Spartan-IIE DLL circuits provide full clock management solution
- Clock generation
  - Synthesizing many clocks from a single reference crystal or clock
- Clock buffering and distribution
  - Providing multiple copies of a single clock
  - SDRAM clocks
- Spread spectrum clocks for EMI reduction
  - DLL circuits allow tolerance for ±2.5% variance

Programmable Solutions Advantages

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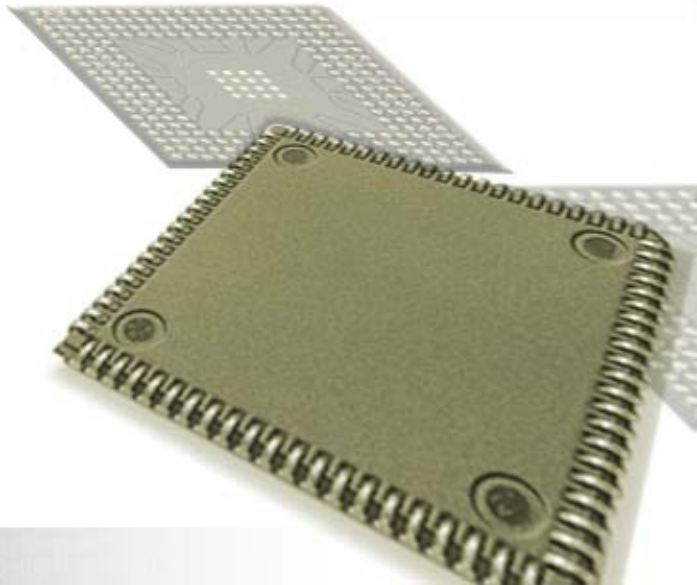


Spartan-IIE Enhances Advantages of Programmable Logic

- Time-to-Market
- Flexibility
- Field Upgradable
- Cost Competitive

Xilinx Programmable Solutions Provide Several Benefits

- Accelerating time-to-market
  - Consumer devices require fast time-to-market
  - ASICs & ASSPs take 12-18 months to spin out
    - Immediate production upon design release
  - Fast design iterations
  - Rich, IP portfolio and efficient tools for design and synthesis
- System integration
- Testing and verification
  - Re-programmable means risk reduction/aversion
  - Solutions are built on a proven FPGA technology with pre-verified silicon and IP that guarantees performance

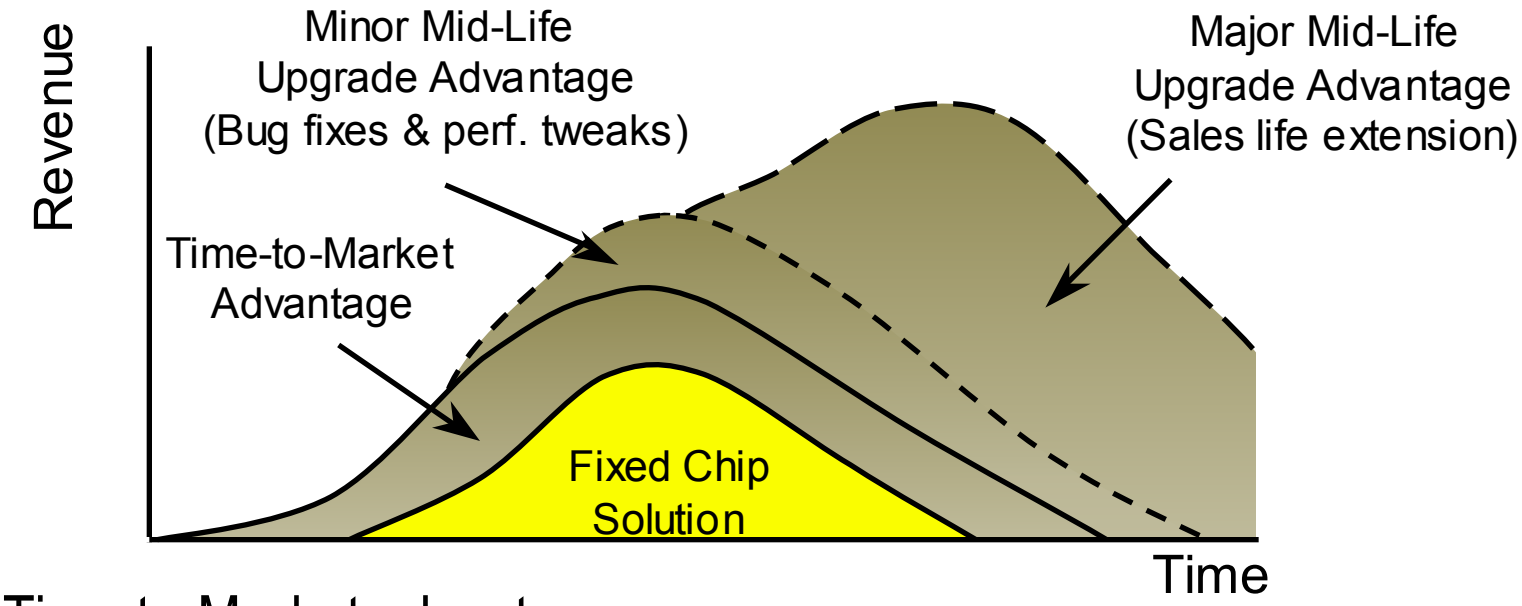
Xilinx Programmable Solutions Provide Several Benefits

- Increased flexibility
  - Product customization to meet customer needs
  - Accommodate multiple standards & spec updates/changes
  - Feature upgrades through field upgradability (IRL)
    - Remote update of software and hardware
    - Increased lifetime for a product (time-in-market) and allows new, interesting applications
    - Enable product features per end user needs
  - Broad product line
  - Broad IP and tools solutions

Xilinx Programmable Solutions Provide Several Advantages

- Issues in creating a stand-alone ASIC/ASSP
  - Which standards and formats will win in which geographies?
  - Choosing the right solution: over-design, under-design
  - Product customization
  - Development cost and amortization
- System cost management and assured source of supply
  - Multiple sourcing for key high $ BOM components
  - Reduced support costs via IRL
  - Commodity component flexibility
  - Programmable logic solutions are standard parts
- Low cost

PLD Development Flow Advantages Accelerating Time-to-Market, Extending Time-in-Market



- Time-to-Market advantage
  - First to market increases market share and revenue advantage
- Time-in-Market advantage
  - Maintains/extends competitive position
  - Can greatly increase life-cycle revenue yield

Xilinx Solutions for D-Cinema

- Projectors with programmable settings for adaptation to environment
- Programmable solutions to new standard adoption/variation
  - Interoperability issues can be overcome with FPGA interfaces
- Programmable cryptography for new algorithms should existing ones be compromised
- Real-time, high-definition image processing available
- Image processing and communications IP speeds design implementation
- Xilinx programmable solutions can differentiate your product from the competition while still conforming to the latest revision of standards
- Faster time-to-market, longer time-in-market